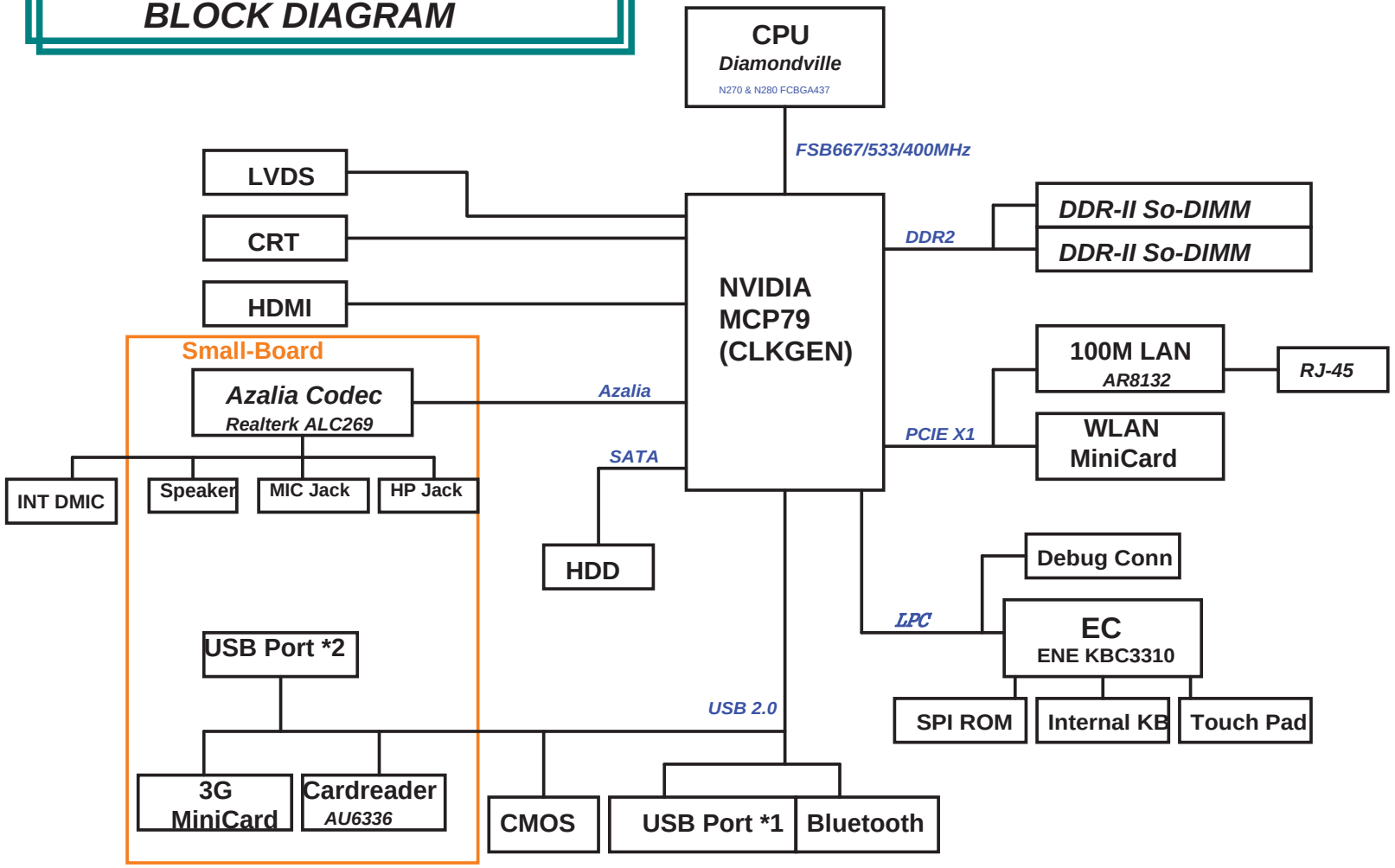
1201I: Diamondville+MCP79 BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : Block Diagram

Engineer: N/A

Size	Project Name	Rev
Custom	1201I	1.0

Date: Monday, July 20, 2009 Sheet 1 of 54

MCP79 GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOSUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOSUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N45	GPIOSUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOSUS3/ USBCC	+VCCP_OV0	I/O CMOS3.3	Sus	VIX-unknown	OFF	output
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	CARD_READER_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F34	GPIO2	SIMCARD_IN#	I/O CMOS3.3	Core	OFF	OFF	iutput
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

<Variant Name>

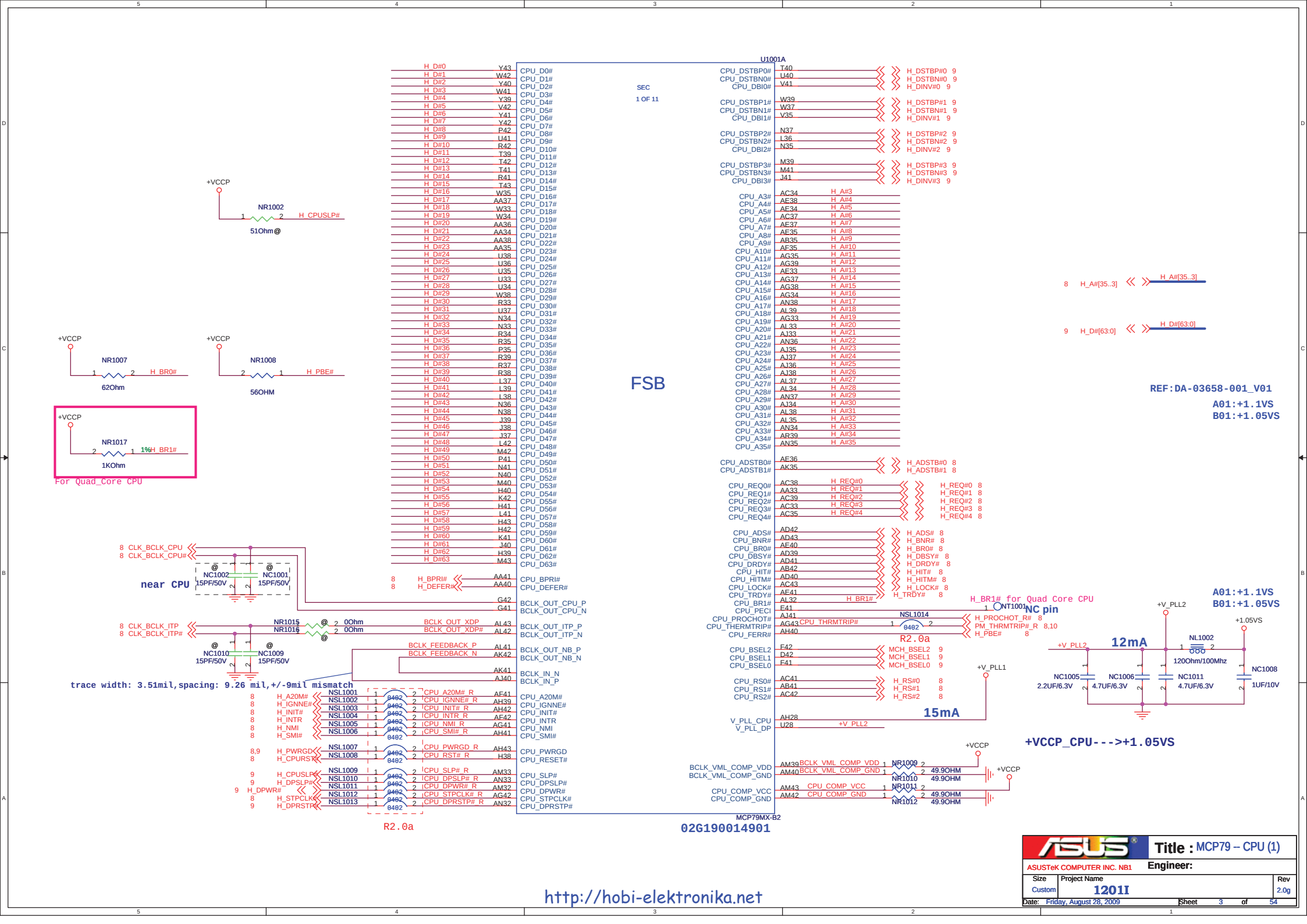
ASUSTek Computer INC.

Title : MCP79 GPIO Setting

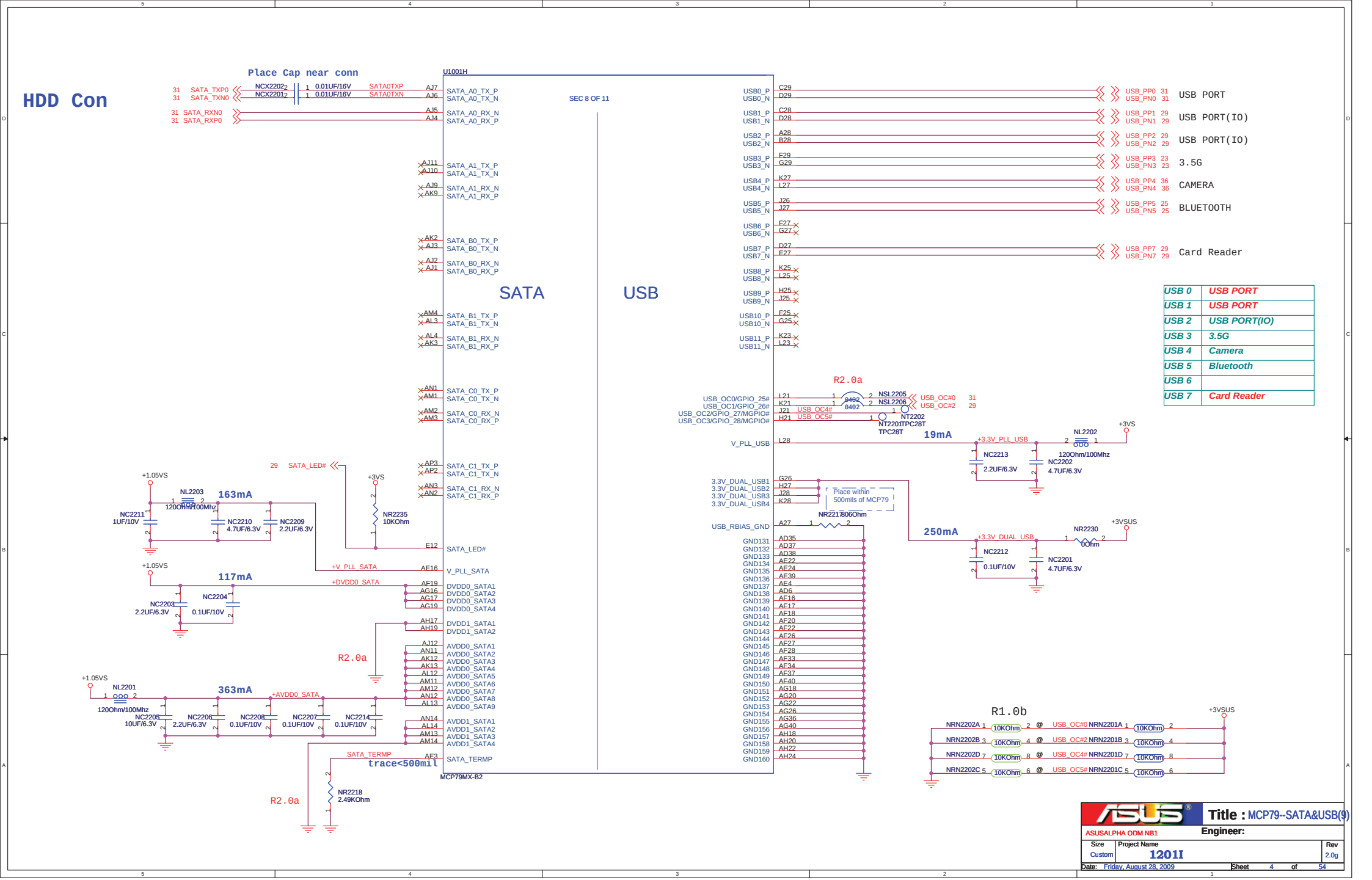
Engineer: N/A

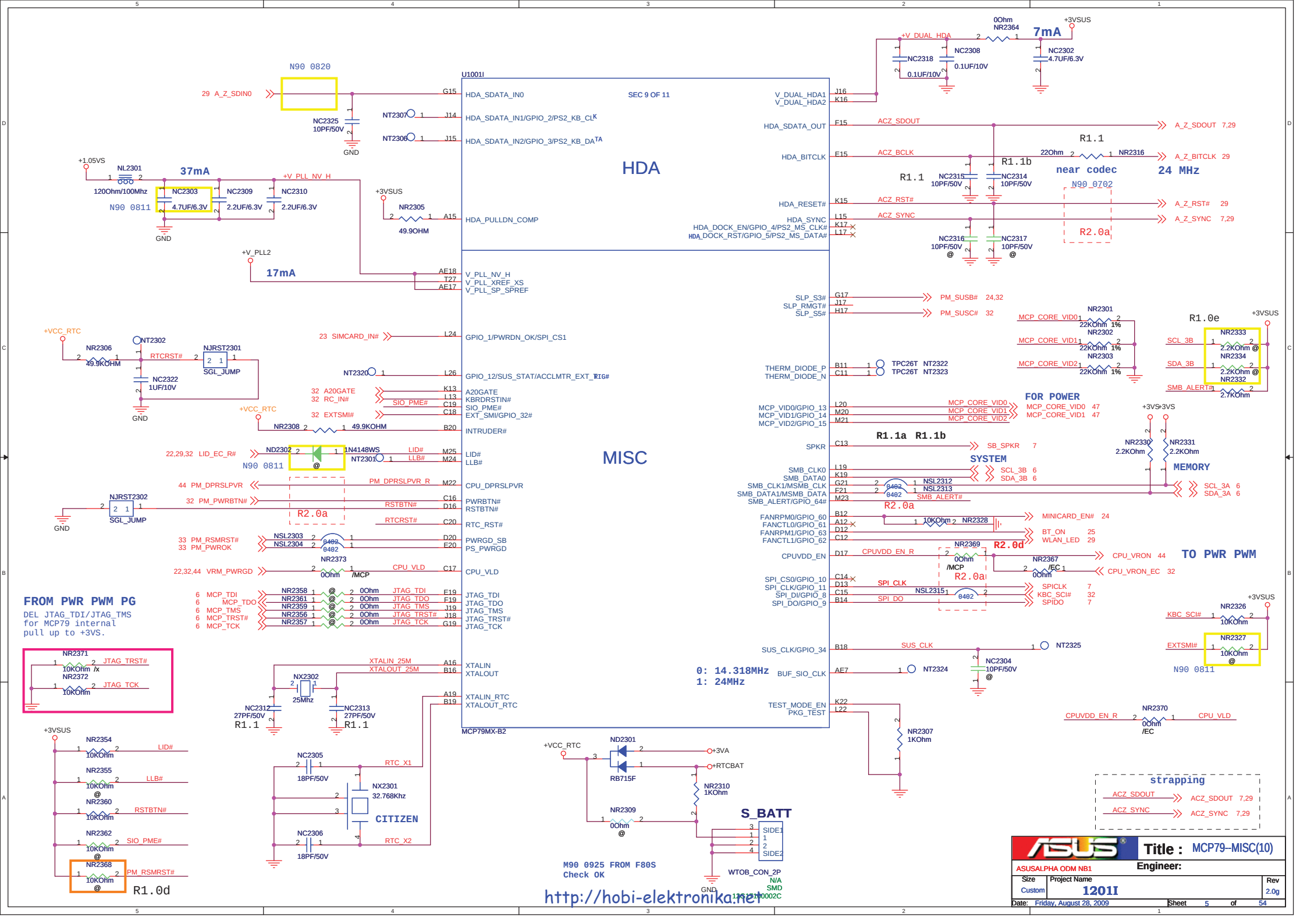
Size	Project Name	Rev
A3	1201I	1.0

Date: Monday, July 20, 2009 Sheet 2 of 54

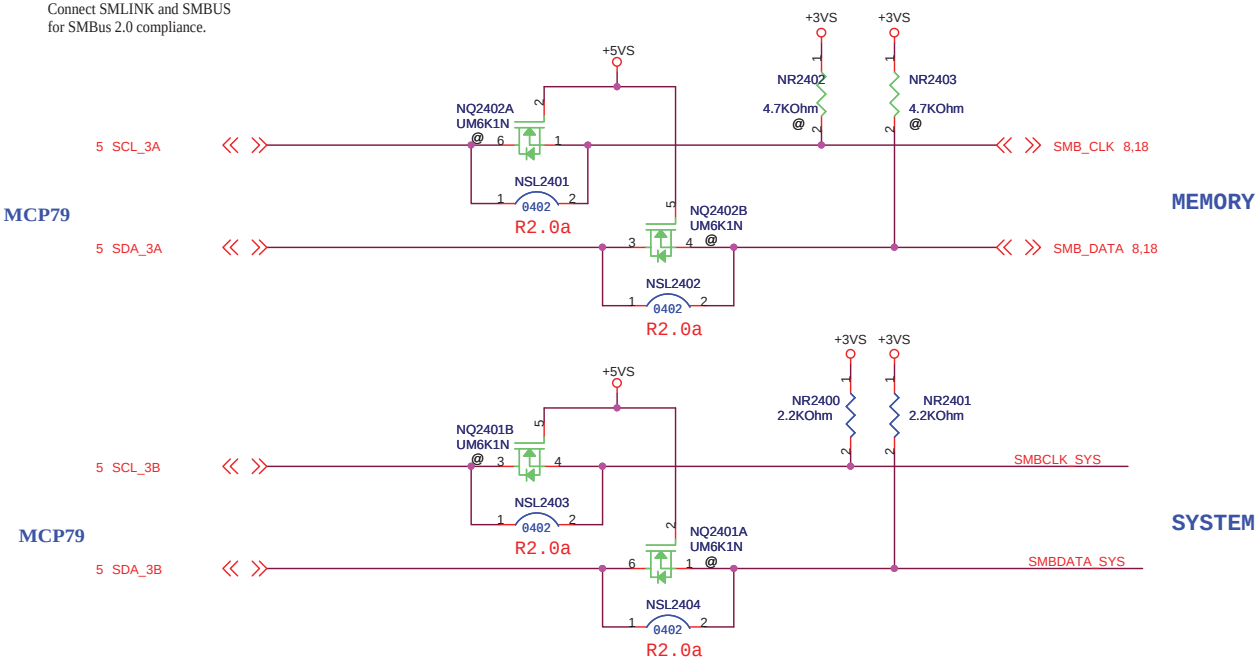


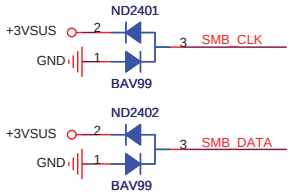
ASUSTeK COMPUTER INC. NB1	Title : MCP79 – CPU (1)	
	Engineer:	
Size: Custom	Project Name: 1201I	Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 3 of 54	



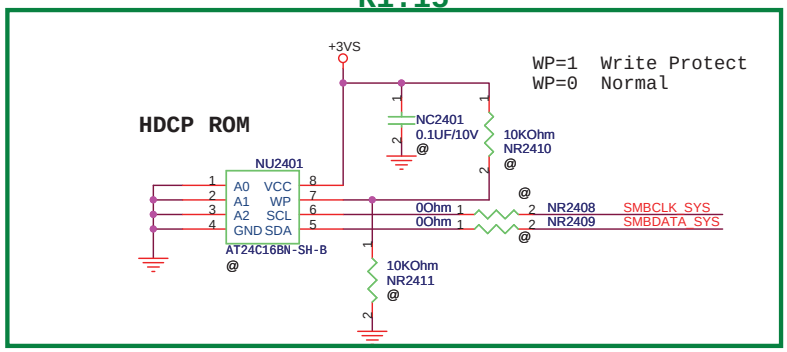

U1001I
MCP79MX-B2
HDA
MISC
SEC 9 OF 11
HDA_SDATA_IN0
HDA_SDATA_IN1/GPIO_2/PS2_KB_CLK
HDA_SDATA_IN2/GPIO_3/PS2_KB_DATA
HDA_PULLDN_COMP
HDA_SDATA_OUT
HDA_BITCLK
HDA_RESET#
HDA_SYNC
HDA_DOCK_EN/GPIO_4/PS2_MS_CLK#
HDA_DOCK_RST/GPIO_5/PS2_MS_DATA#
V_PLL_NV_H
V_PLL_XREF_XS
V_PLL_SP_SPREF
GPIO_1/PWRDN_OK/SPI_CS1
GPIO_12/SUS_STAT/ACCLMTR_EXT_INT#
A20GATE
KBRDRSTIN#
SIO_PME#
EXT_SMI/GPIO_32#
INTRUDER#
LID#
LLB#
CPU_DPRSLPVR
PWRBTN#
RSTBTN#
RTC_RST#
PWRGD_SB
PS_PWRGD
CPU_VLD
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST#
JTAG_TCK
XTALIN
XTALOUT
XTALIN_RTC
XTALOUT_RTC
V_DUAL_HDA1
V_DUAL_HDA2
SLP_S3#
SLP_RMGT#
SLP_S5#
THERM_DIODE_P
THERM_DIODE_N
MCP_VID0/GPIO_13
MCP_VID1/GPIO_14
MCP_VID2/GPIO_15
SPKR
SMB_CLK0
SMB_DATA0
SMB_CLK1/MSMB_CLK
SMB_DATA1/MSMB_DATA
SMB_ALERT/GPIO_64#
FANRPM0/GPIO_60
FANCTL0/GPIO_61
FANRPM1/GPIO_63
FANCTL1/GPIO_62
CPUVDD_EN
SPI_CS0/GPIO_10
SPI_CLK/GPIO_11
SPI_DI/GPIO_8
SPI_DO/GPIO_9
SUS_CLK/GPIO_34
BUF_SIO_CLK
TEST_MODE_EN
PKG_TEST
0: 14.318MHz
1: 24MHz
N90 0820
N90 0811
N90 0702
R1.1
R1.1b
near codec
24 MHz
R1.0e
R1.1a R1.1b
R2.0a
R2.0d
FOR POWER
SYSTEM
MEMORY
TO PWR PWM
FROM PWR PWM PG
DEL JTAG_TDI/JTAG_TMS
for MCP79 internal
pull up to +3VS.
R1.0d
strapping
ACZ_SDOUT
ACZ_SYNC
S_BATT
CITIZEN
M90 0925 FROM F80S
Check OK
http://hobi-elektronika.net
ASUSALPHA ODM NB1
Title : MCP79--MISC(10)
Engineer:
Size Custom
Project Name 1201I
Rev 2.0g
Date: Friday, August 28, 2009
Sheet 5 of 54

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

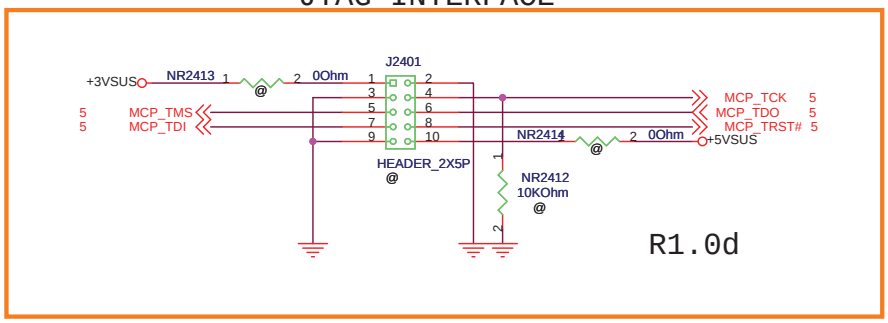




R1.15



JTAG INTERFACE



ASUSTeK COMPUTER INC	Title : HDCP and Other	
	Engineer:	
Size: B	Project Name: 1201I	Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 6 of 54	

HDA_SYNC STRAP (BUF_SIO_CLK)	
0	14.318MHz (default)
1	24MHz

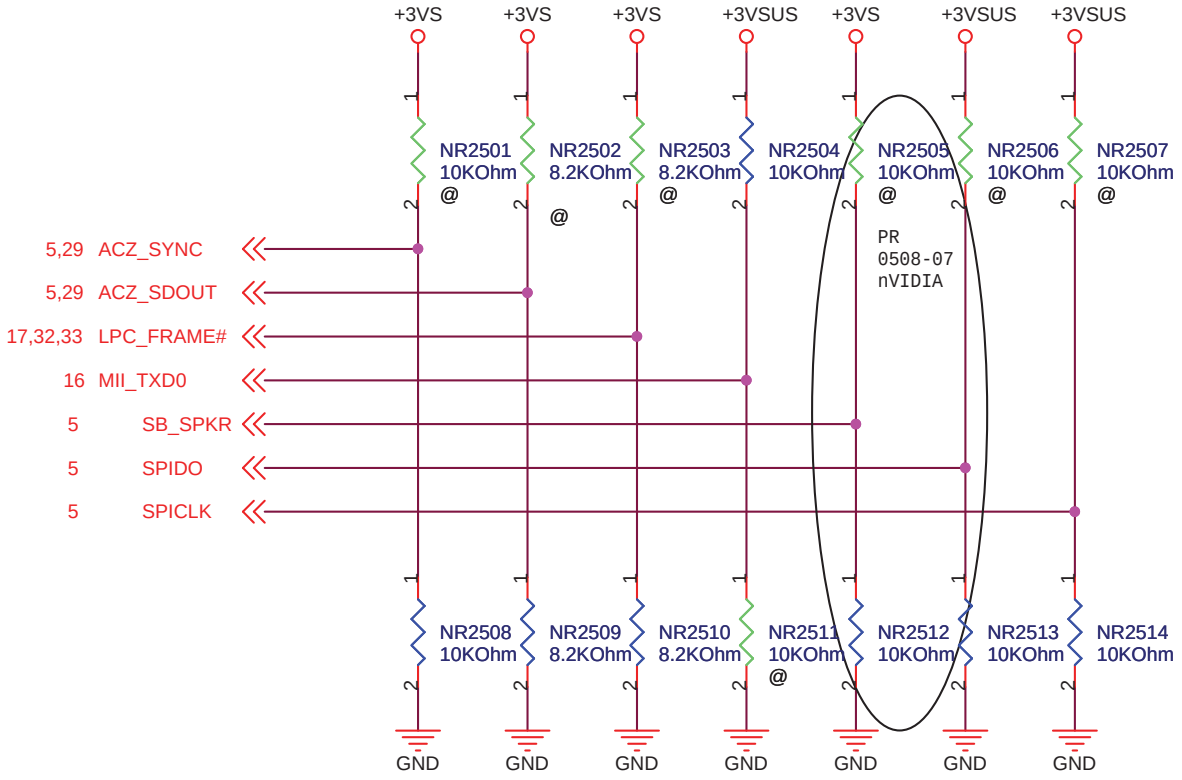
RGMII_TXD0	
0	MII
1	RGMII

SPKR	
0	User mode boot Init table
1	Safe mode boot Init table

Base on EC

HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz



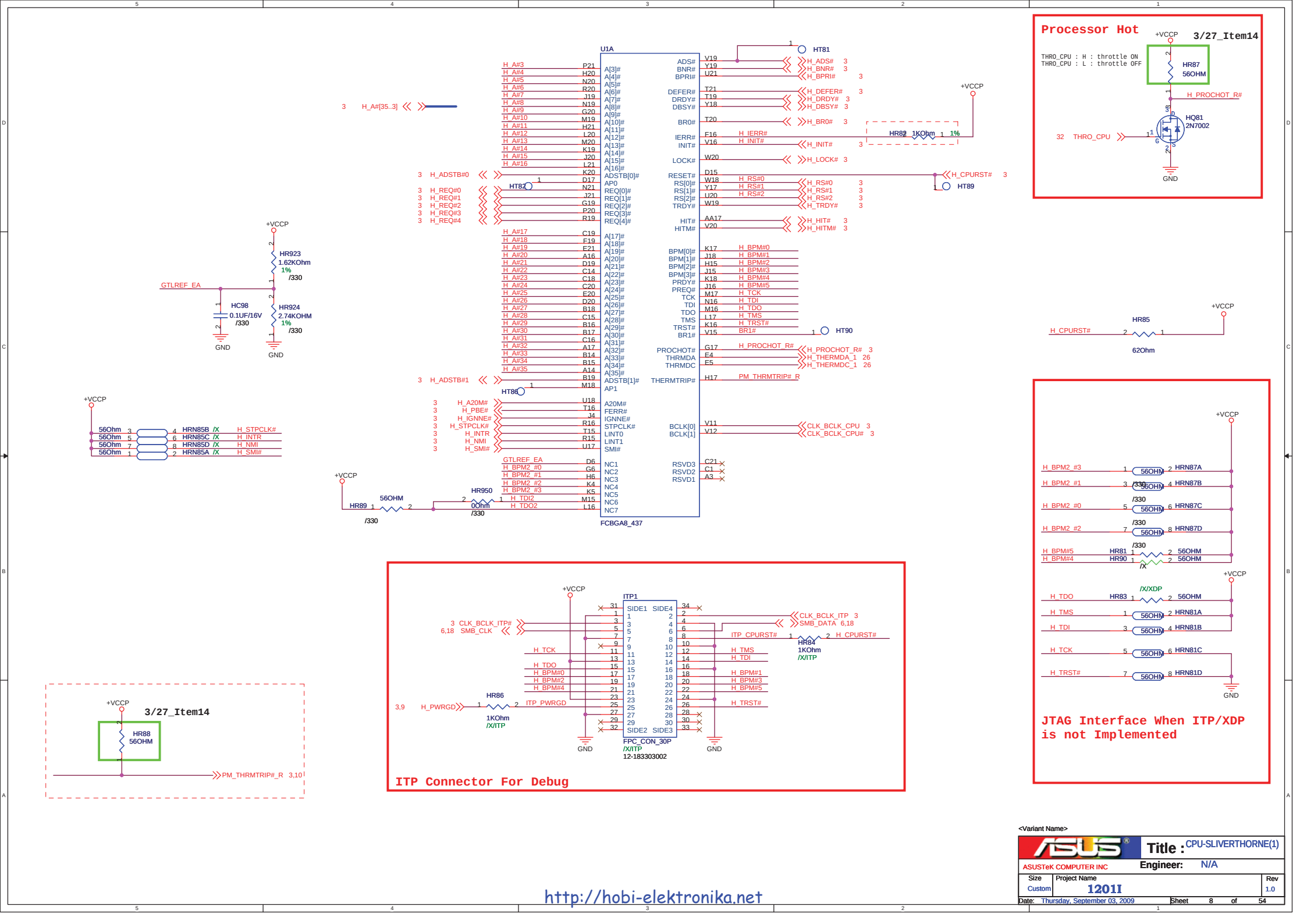
Title : MCP79 STRAP

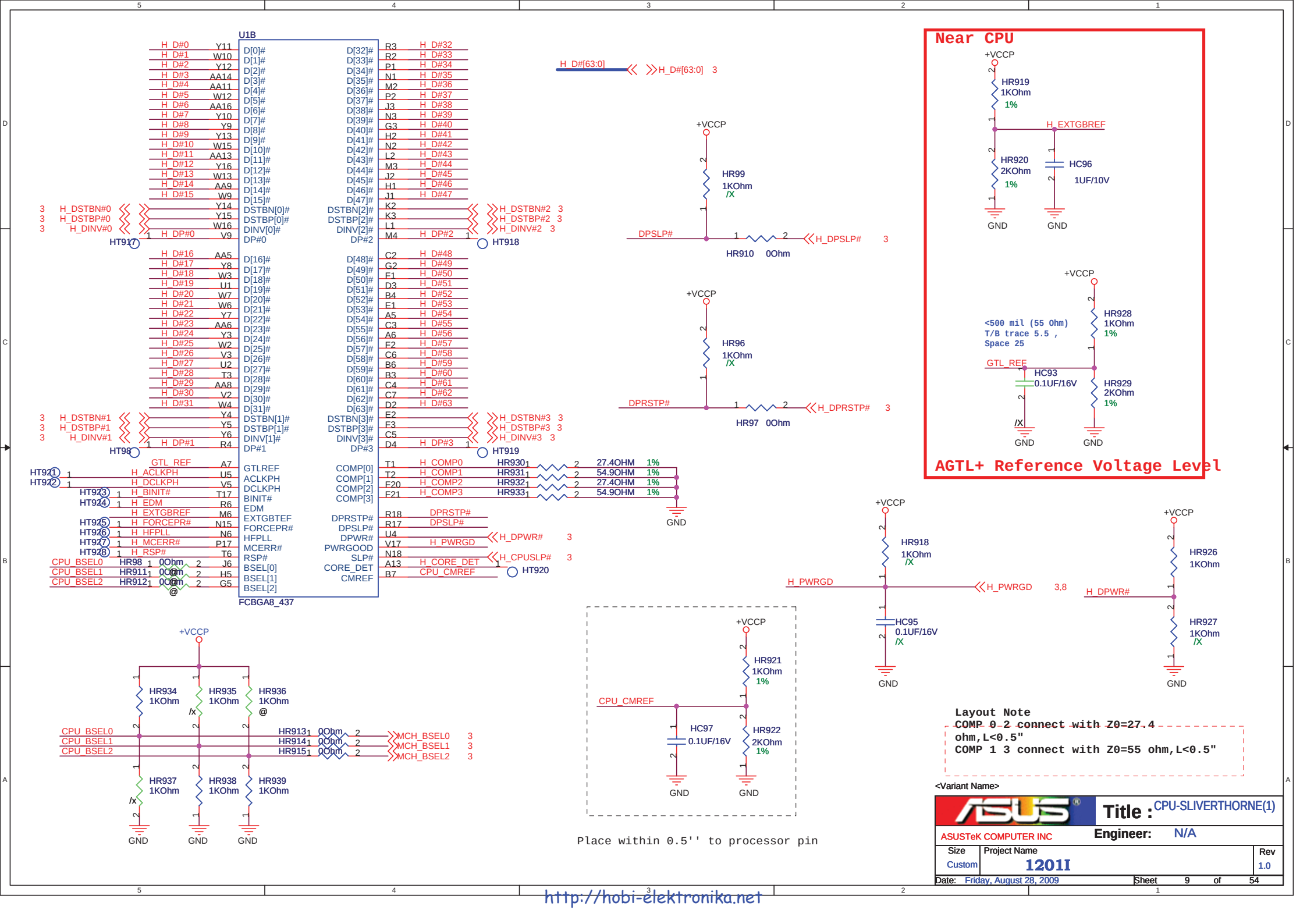
ASUSTeK COMPUTER INC. NB1

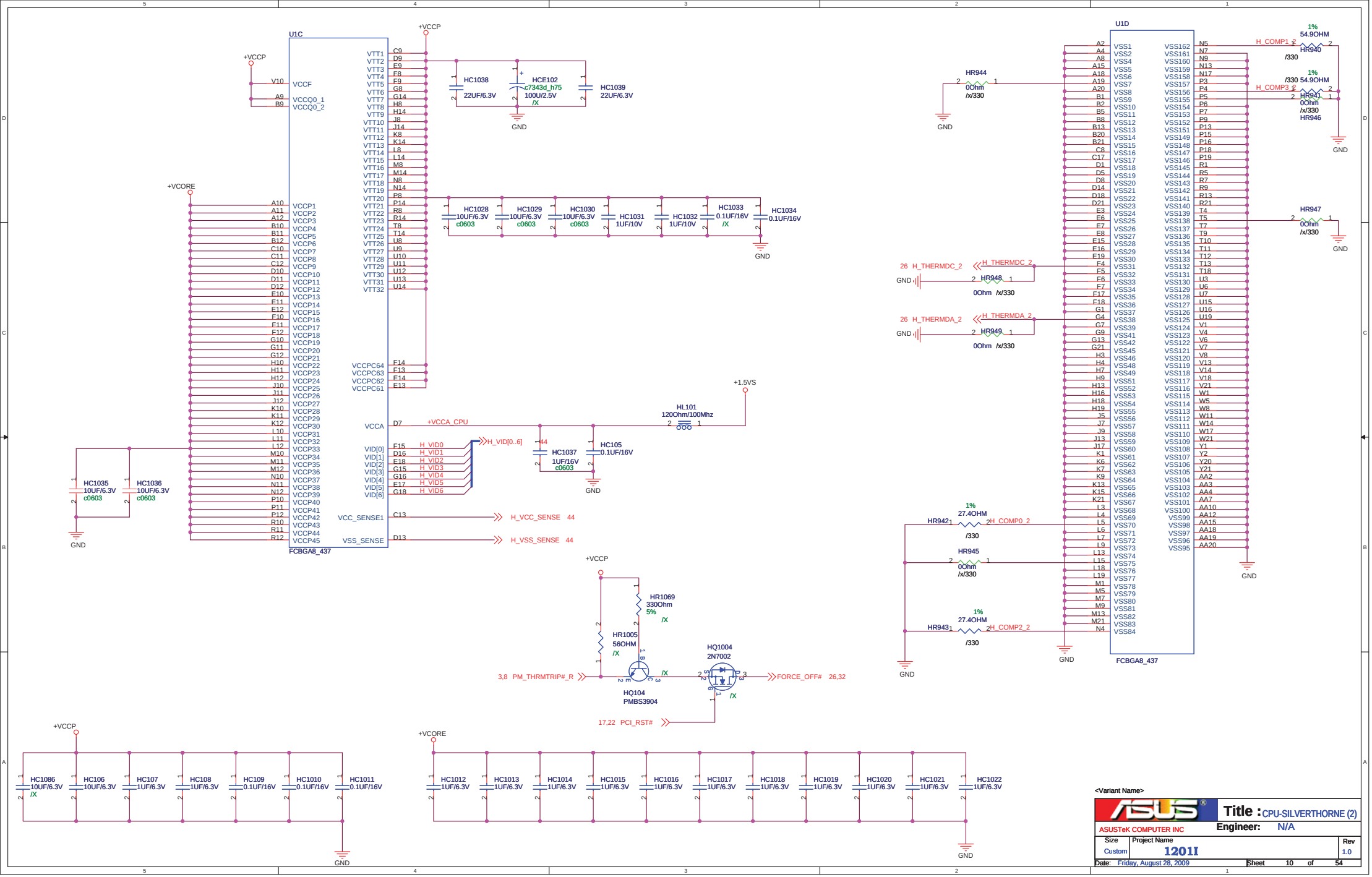
Engineer:

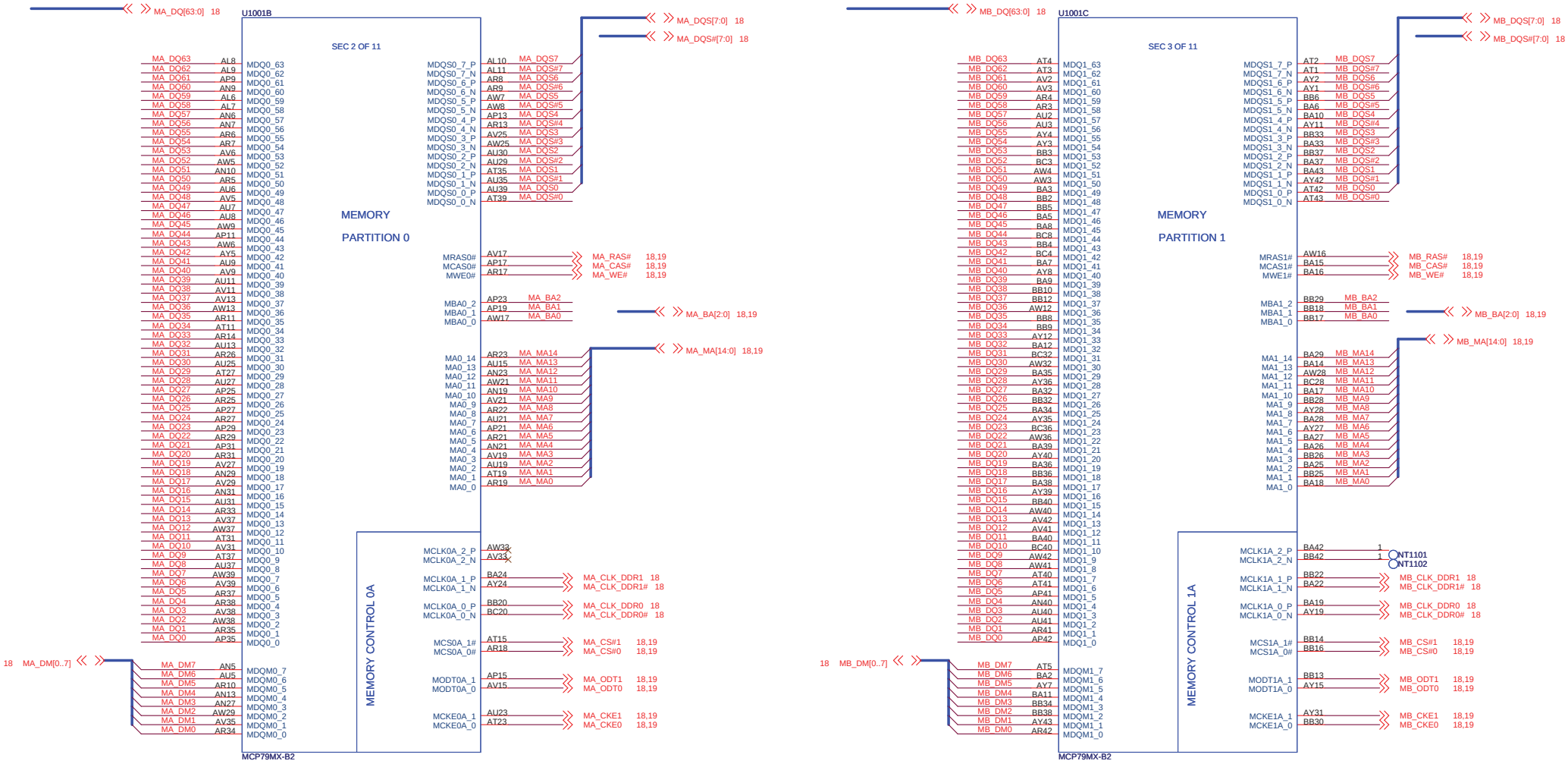
Size	Project Name	Rev
A	1201I	2.0g

Date: Friday, August 28, 2009 Sheet 7 of 54

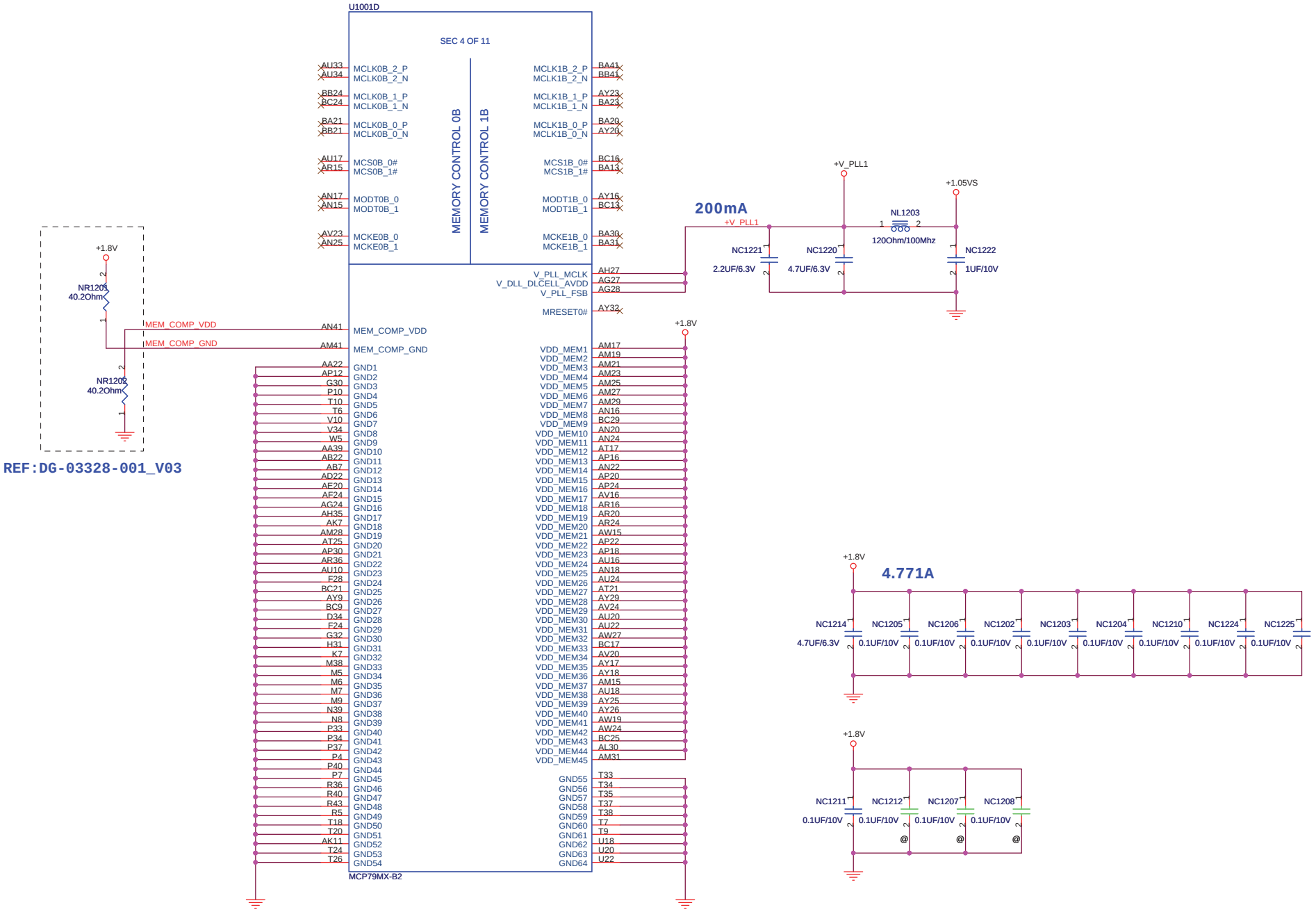




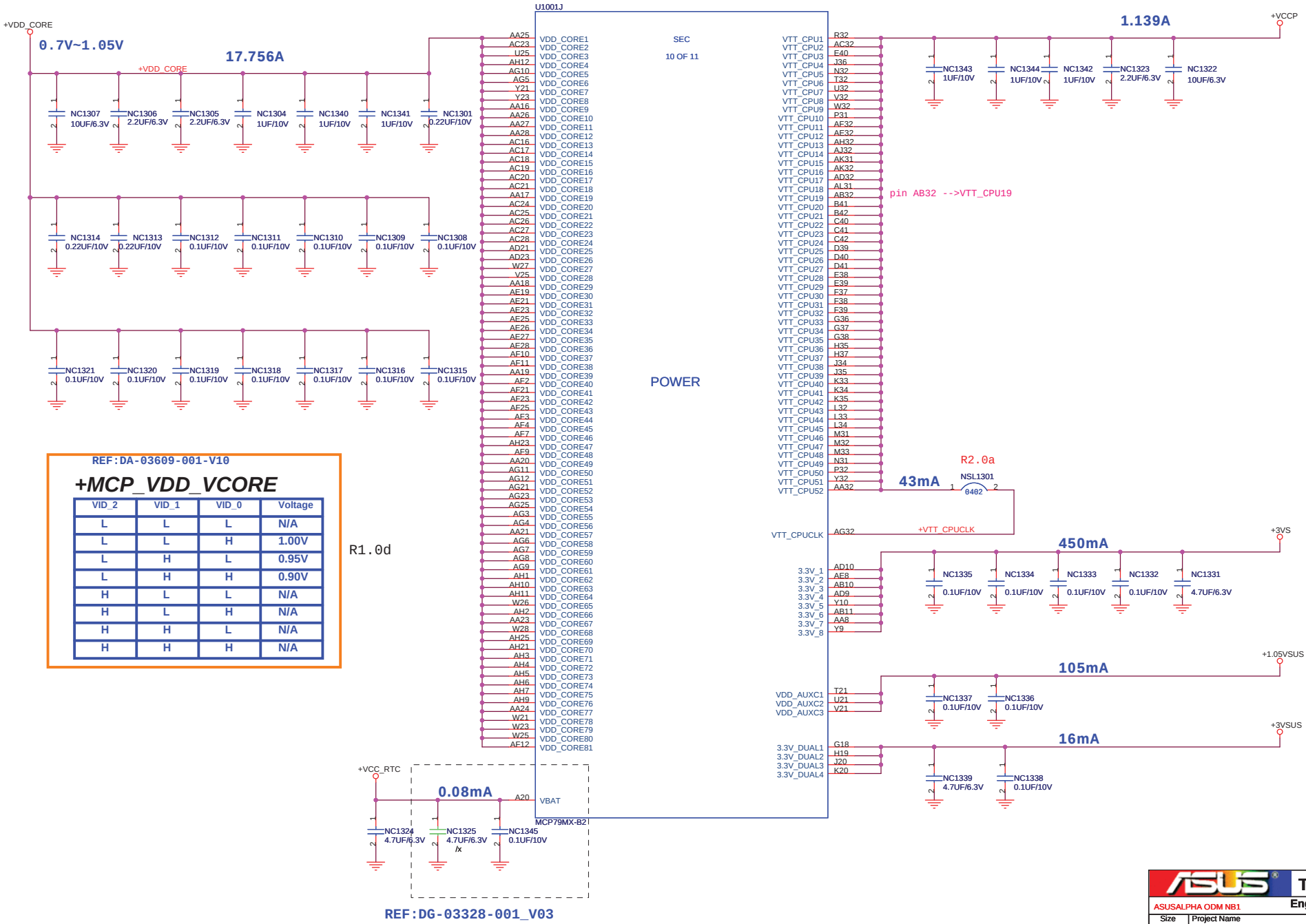


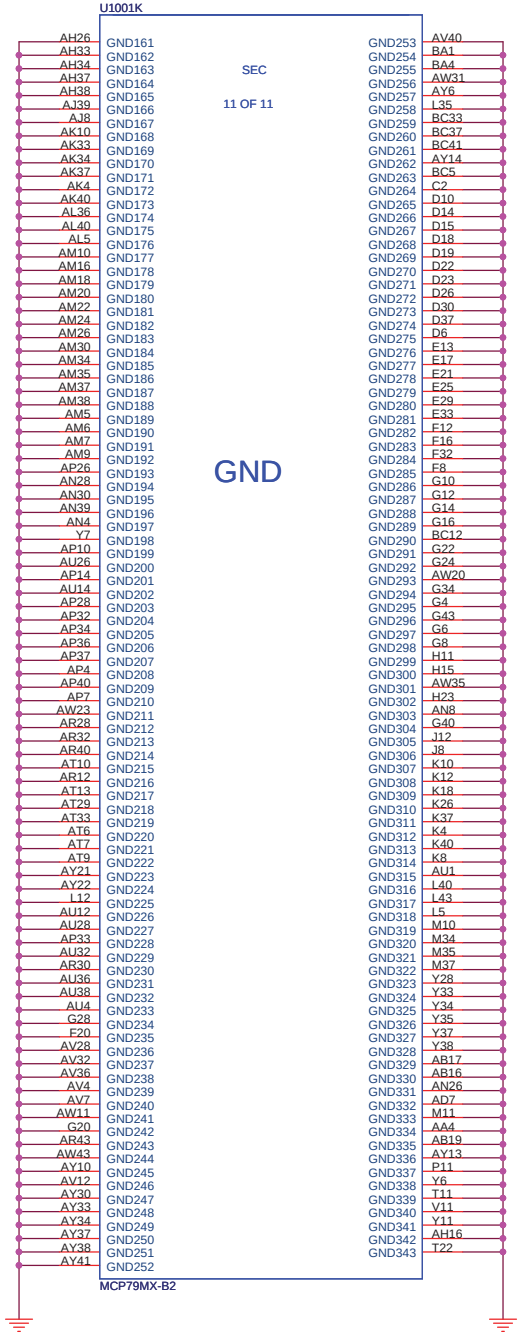


ASUSTeK COMPUTER INC. NB1	Title : MCP79-DDR2 BUS(2)		
	Engineer:		
Size: Custom	Project Name: 1201I		Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 11 of 54		

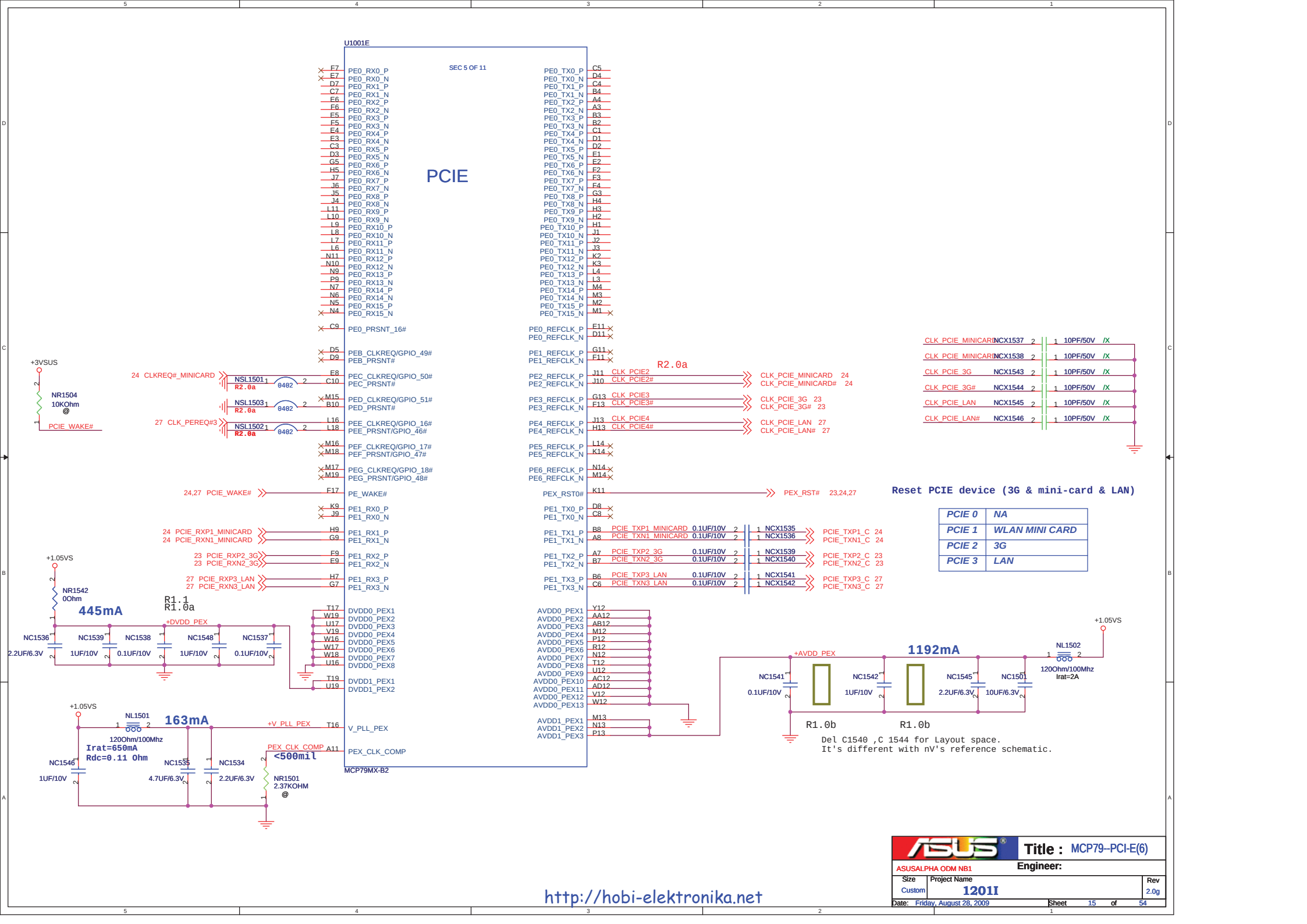


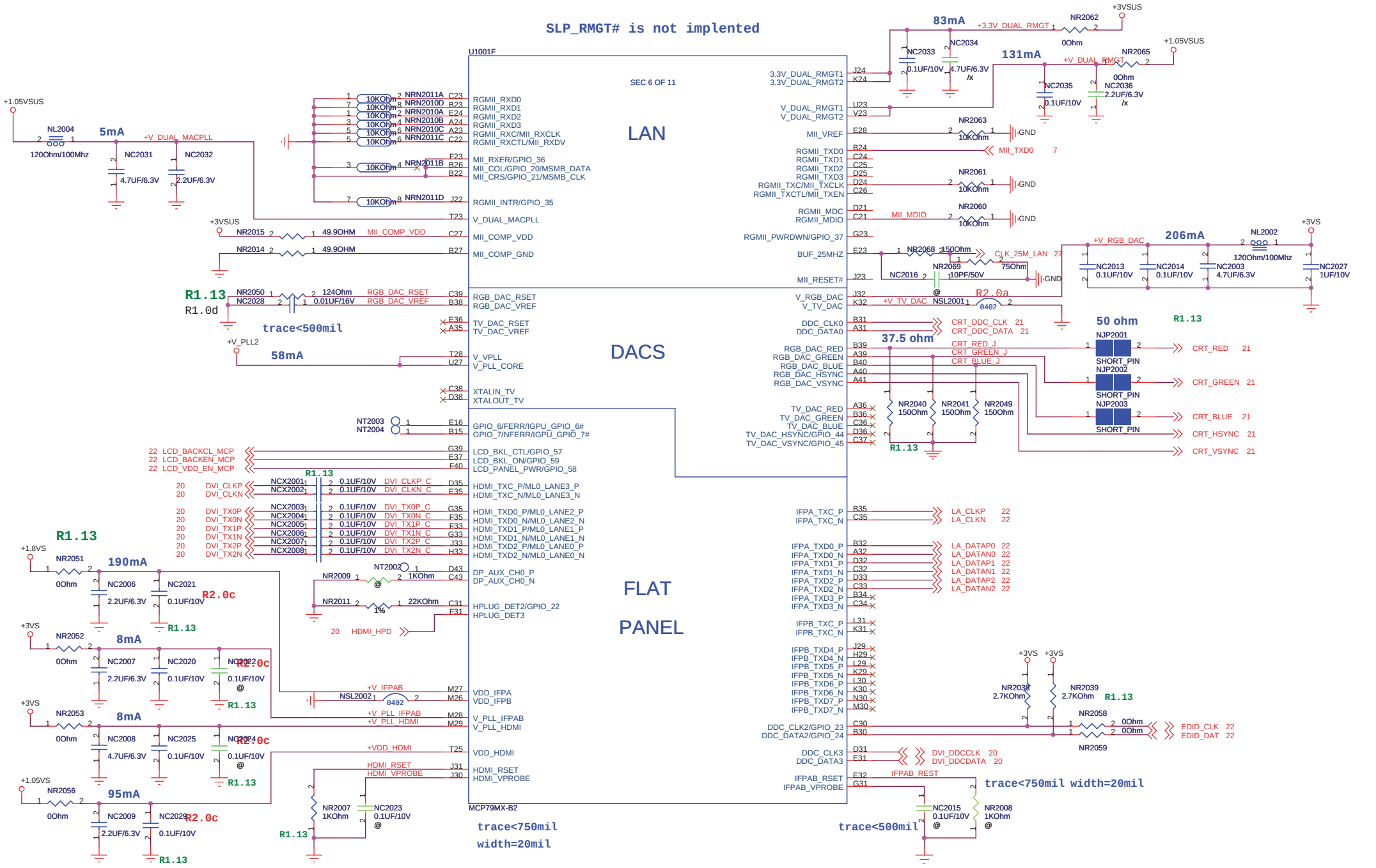
Title : MCP79-MEM CNTL(3)		
ASUSALPHA ODM NB1	Engineer:	
Size: A3	Project Name: 1201I	Rev: 2.0g
Date: Tuesday, August 04, 2009	Sheet 12 of 54	



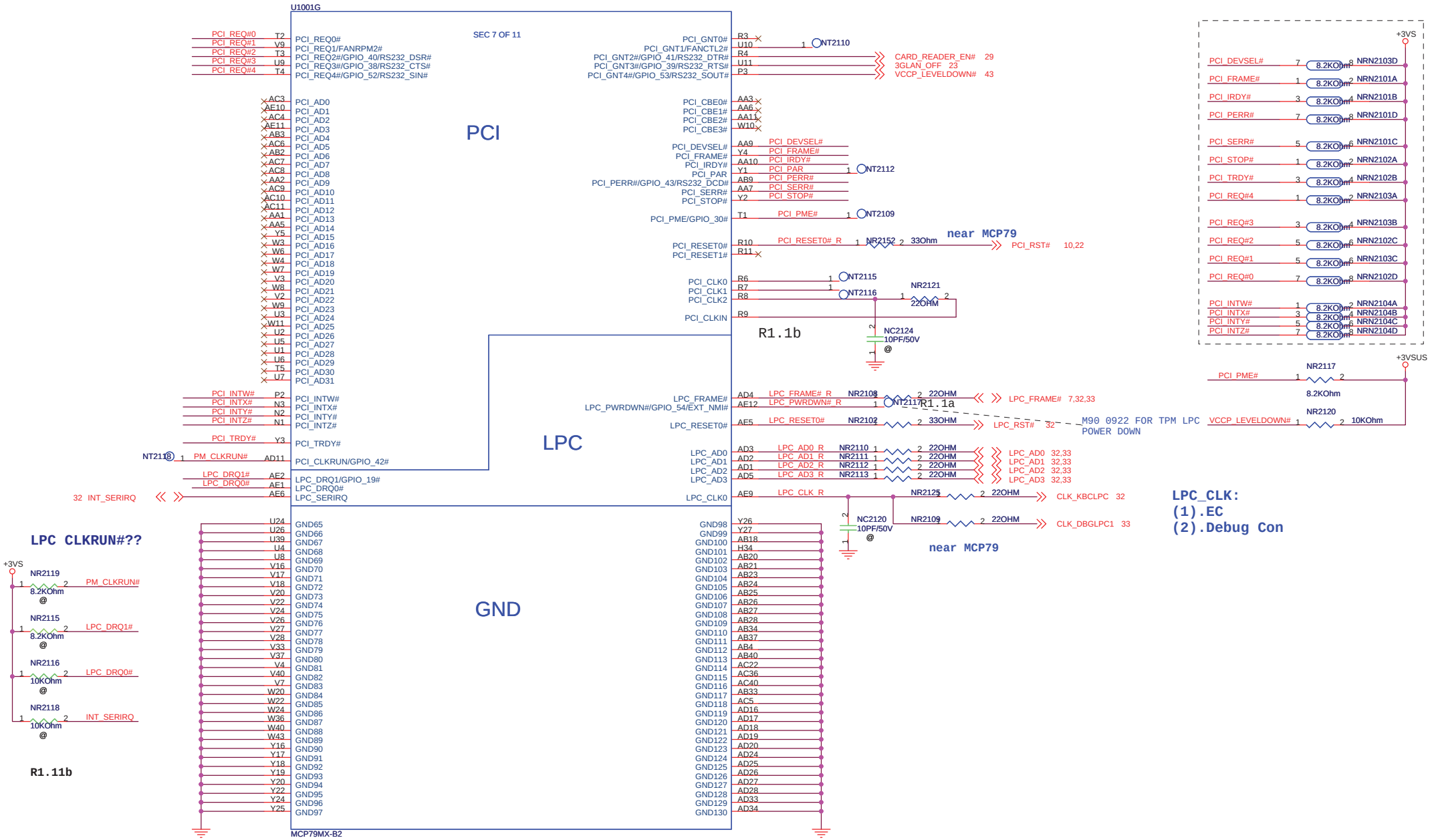


ASUSALPHA ODM NB1	Title : MCP79--GND(5)	
	Engineer:	
Size: A3	Project Name: 1201I	Rev: 2.0g
Date: Monday, July 20, 2009	Sheet 14 of 54	

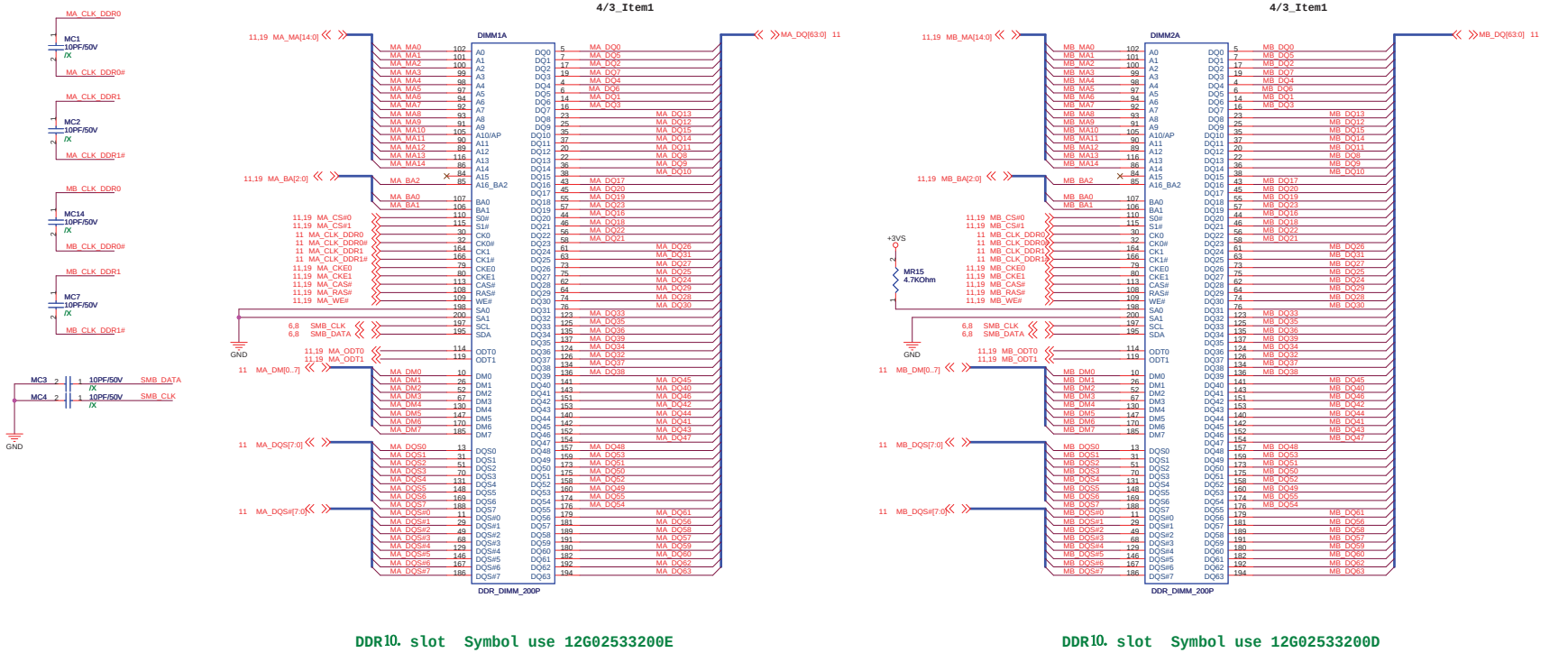

U1001E
SEC 5 OF 11
PCIE
MCP79MX-B2
PE0_RX0_P
PE0_RX0_N
PE0_RX1_P
PE0_RX1_N
PE0_RX2_P
PE0_RX2_N
PE0_RX3_P
PE0_RX3_N
PE0_RX4_P
PE0_RX4_N
PE0_RX5_P
PE0_RX5_N
PE0_RX6_P
PE0_RX6_N
PE0_RX7_P
PE0_RX7_N
PE0_RX8_P
PE0_RX8_N
PE0_RX9_P
PE0_RX9_N
PE0_RX10_P
PE0_RX10_N
PE0_RX11_P
PE0_RX11_N
PE0_RX12_P
PE0_RX12_N
PE0_RX13_P
PE0_RX13_N
PE0_RX14_P
PE0_RX14_N
PE0_RX15_P
PE0_RX15_N
PE0_TX0_P
PE0_TX0_N
PE0_TX1_P
PE0_TX1_N
PE0_TX2_P
PE0_TX2_N
PE0_TX3_P
PE0_TX3_N
PE0_TX4_P
PE0_TX4_N
PE0_TX5_P
PE0_TX5_N
PE0_TX6_P
PE0_TX6_N
PE0_TX7_P
PE0_TX7_N
PE0_TX8_P
PE0_TX8_N
PE0_TX9_P
PE0_TX9_N
PE0_TX10_P
PE0_TX10_N
PE0_TX11_P
PE0_TX11_N
PE0_TX12_P
PE0_TX12_N
PE0_TX13_P
PE0_TX13_N
PE0_TX14_P
PE0_TX14_N
PE0_TX15_P
PE0_TX15_N
PE0_PRSNT_16#
PEB_CLKREQ/GPIO_49#
PEB_PRSNT#
PEC_CLKREQ/GPIO_50#
PEC_PRSNT#
PED_CLKREQ/GPIO_51#
PED_PRSNT#
PEE_CLKREQ/GPIO_16#
PEE_PRSNT/GPIO_46#
PEF_CLKREQ/GPIO_17#
PEF_PRSNT/GPIO_47#
PEG_CLKREQ/GPIO_18#
PEG_PRSNT/GPIO_48#
PE_WAKE#
PE1_RX0_P
PE1_RX0_N
PE1_RX1_P
PE1_RX1_N
PE1_RX2_P
PE1_RX2_N
PE1_RX3_P
PE1_RX3_N
PE0_REFCLK_P
PE0_REFCLK_N
PE1_REFCLK_P
PE1_REFCLK_N
PE2_REFCLK_P
PE2_REFCLK_N
PE3_REFCLK_P
PE3_REFCLK_N
PE4_REFCLK_P
PE4_REFCLK_N
PE5_REFCLK_P
PE5_REFCLK_N
PE6_REFCLK_P
PE6_REFCLK_N
PEX_RST0#
PE1_TX0_P
PE1_TX0_N
PE1_TX1_P
PE1_TX1_N
PE1_TX2_P
PE1_TX2_N
PE1_TX3_P
PE1_TX3_N
DVDD0_PEX1
DVDD0_PEX2
DVDD0_PEX3
DVDD0_PEX4
DVDD0_PEX5
DVDD0_PEX6
DVDD0_PEX7
DVDD0_PEX8
DVDD1_PEX1
DVDD1_PEX2
V_PLL_PEX
PEX_CLK_COMP
AVDD0_PEX1
AVDD0_PEX2
AVDD0_PEX3
AVDD0_PEX4
AVDD0_PEX5
AVDD0_PEX6
AVDD0_PEX7
AVDD0_PEX8
AVDD0_PEX9
AVDD0_PEX10
AVDD0_PEX11
AVDD0_PEX12
AVDD0_PEX13
AVDD1_PEX1
AVDD1_PEX2
AVDD1_PEX3
R2.0a
CLK_PCIE2
CLK_PCIE2#
CLK_PCIE3
CLK_PCIE3#
CLK_PCIE4
CLK_PCIE4#
CLK_PCIE_MINICARD 24
CLK_PCIE_MINICARD# 24
CLK_PCIE_3G 23
CLK_PCIE_3G# 23
CLK_PCIE_LAN 27
CLK_PCIE_LAN# 27
PEX_RST# 23,24,27
24 CLKREQ#_MINICARD
27 CLK_PEREQ#3
NSL1501
NSL1503
NSL1502
0402
+3VSUS
NR1504
10KOhm
@
PCIE_WAKE#
24,27 PCIE_WAKE#
24 PCIE_RXP1_MINICARD
24 PCIE_RXN1_MINICARD
23 PCIE_RXP2_3G
23 PCIE_RXN2_3G
27 PCIE_RXP3_LAN
27 PCIE_RXN3_LAN
PCIE_TXP1_MINICARD 0.1UF/10V
PCIE_TXN1_MINICARD 0.1UF/10V
PCIE_TXP2_3G 0.1UF/10V
PCIE_TXN2_3G 0.1UF/10V
PCIE_TXP3_LAN 0.1UF/10V
PCIE_TXN3_LAN 0.1UF/10V
NCX1535
NCX1536
NCX1539
NCX1540
NCX1541
NCX1542
PCIE_TXP1_C 24
PCIE_TXN1_C 24
PCIE_TXP2_C 23
PCIE_TXN2_C 23
PCIE_TXP3_C 27
PCIE_TXN3_C 27
CLK_PCIE_MINICARD NCX1537 10PF/50V /X
CLK_PCIE_MINICARD# NCX1538 10PF/50V /X
CLK_PCIE_3G NCX1543 10PF/50V /X
CLK_PCIE_3G# NCX1544 10PF/50V /X
CLK_PCIE_LAN NCX1545 10PF/50V /X
CLK_PCIE_LAN# NCX1546 10PF/50V /X
Reset PCIE device (3G & mini-card & LAN)
PCIE 0 NA
PCIE 1 WLAN MINI CARD
PCIE 2 3G
PCIE 3 LAN
+1.05VS
NR1542
0Ohm
445mA
R1.1
R1.0a
+DVDD_PEX
NC1536 2.2UF/6.3V
NC1539 1UF/10V
NC1538 0.1UF/10V
NC1548 1UF/10V
NC1537 0.1UF/10V
+1.05VS
NL1501
163mA
120Ohm/100Mhz
Irat=650mA
Rdc=0.11 Ohm
+V_PLL_PEX
NC1546 1UF/10V
NC1535 4.7UF/6.3V
NC1534 2.2UF/6.3V
PEX_CLK_COMP
<500mil
NR1501
2.37KOHM
@
+AVDD_PEX
1192mA
NC1541 0.1UF/10V
NC1542 1UF/10V
NC1545 2.2UF/6.3V
NC1501 10UF/6.3V
+1.05VS
NL1502
120Ohm/100Mhz
Irat=2A
R1.0b
R1.0b
Del C1540 ,C 1544 for Layout space.
It's different with nV's reference schematic.
ASUSALPHA ODM NB1
Title : MCP79--PCI-E(6)
Engineer:
Size Custom
Project Name 1201I
Rev 2.0g
Date: Friday, August 28, 2009
Sheet 15 of 54
http://hobi-elektronika.net

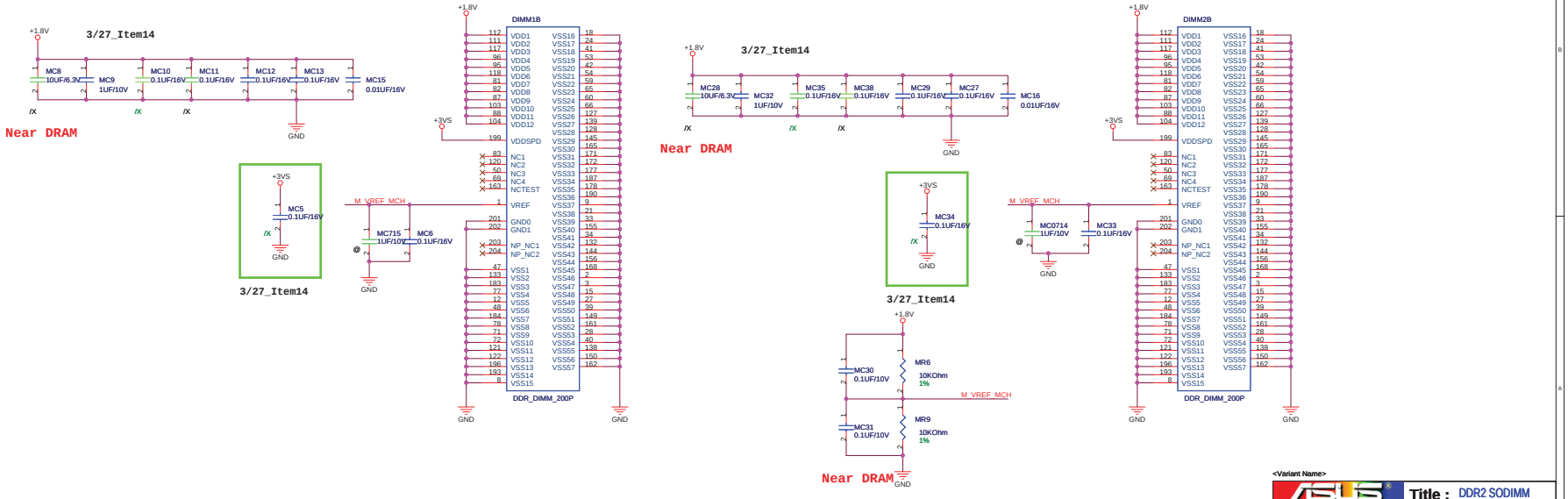


Title :	MCP79--LAN (7)
ASUSALPHA ODM NB1	Engineer:
Size: A3	Project Name: 1201I
Rev: 2.0g	
Date: Wednesday, September 02, 2009	Sheet 16 of 54



ASUSALPHA ODM NB1	Title : MCP79--LPC (8)	
	Engineer:	
Size: A3	Project Name: 1201I	Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 17 of 54	





+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve STR_EN# and SUSC#

HAS TO BE SWAPED

M_A_A14 is reserved signal and keep R0901 separately

Don't include this page into DesignIP because of swapping

MA_MA[14:0] 11,18
MA_BA[2:0] 11,18
MA_CAS# 11,18
MA_RAS# 11,18
MA_WE# 11,18

MB_MA[14:0] 11,18
MB_BA[2:0] 11,18
MB_CAS# 11,18
MB_RAS# 11,18
MB_WE# 11,18

+VTTDDR

MC0908 MC0905 MC0915 MC0916 MC0910 MC0913 MC0904 MC0911 MC0914 MC0907 MC0909 MC0912 MC0906
0.1UF/10V

GND

Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

+VTTDDR

MC0917 MC0924 MC0925 MC0923 MC0921 MC0928 MC0926 MC0927 MC0920 MC0919 MC0922 MC0929 MC0918
0.1UF/10V

+1.8V

16X0.1UF to GND

16X0.1UF to 1.8V

R1.0f

+VTTDDR

47Ohm MR0907 MA_CKE1 11,18

47Ohm MRN0905H MB_ODT1 11,18
47Ohm MRN0905G MB_CS#1 11,18
47Ohm MRN0905E MB_CAS#

47Ohm MRN0905F MB_WE#
47Ohm MRN0906F MB_BA0
47Ohm MRN0906G MB_MA10

47Ohm MRN0901A MA_CKE0 11,18 R1.0d
47Ohm MRN0903B MA_MA6
47Ohm MRN0901G MA_MA7
47Ohm MRN0901D MA_MA9
47Ohm MRN0901C MA_MA12
47Ohm MRN0901F MA_MA8

47Ohm MRN0903G MA_MA0
47Ohm MRN0903H MA_BA1
47Ohm MRN0903D MA_MA10
47Ohm MRN0902A MA_RAS#
47Ohm MRN0902C MA_MA13

47Ohm MRN0902H MA_ODT1 11,18 R1.0d

47Ohm MR0902 MA_MA14 R1.0d
47Ohm MR0908 MA_CS#0 11,18 R1.0d
R1.0d
R1.0d

47Ohm MRN0909D MB_CKE0 11,18

47Ohm MRN0905B MB_MA13
47Ohm MRN0905C MB_ODT0 11,18
47Ohm MRN0906H MB_CS#0 11,18
47Ohm MRN0906C MB_BA1
47Ohm MRN0905D MB_RAS#

47Ohm MRN0903A MA_MA3
47Ohm MRN0901E MA_MA5
47Ohm MRN0902G MA_CS#1 11,18 R1.0d
47Ohm MRN0901H MA_MA11 R1.0d
47Ohm MRN0901B MA_BA2
47Ohm MRN0903F MA_MA2
47Ohm MRN0903C MA_MA4

47Ohm MRN0906D MB_MA0
47Ohm MRN0906B MB_MA2
47Ohm MRN0906A MB_MA4
47Ohm MRN0907G MB_MA8
47Ohm MRN0906E MB_MA1
47Ohm MRN0907H MB_MA3
47Ohm MRN0907C MB_MA6
47Ohm MRN0907F MB_MA5

47Ohm MRN0909F MB_BA2
47Ohm MRN0907A MB_MA9
47Ohm MRN0909H MB_MA14
47Ohm MRN0909G MB_MA12
47Ohm MRN0907E MB_MA7
47Ohm MRN0907D MB_MA11

47Ohm MRN0903E MA_MA1

47Ohm MRN0902B MA_BA0
47Ohm MRN0902E MA_WE#
47Ohm MRN0902F MA_CAS#
47Ohm MRN0902D MA_ODT0 11,18 R1.0d

47Ohm MRN0909B
47Ohm MRN0905A

47Ohm MRN0909E MB_CKE1 11,18
47Ohm MRN0909A

47Ohm MRN0909C
47Ohm MRN0907B

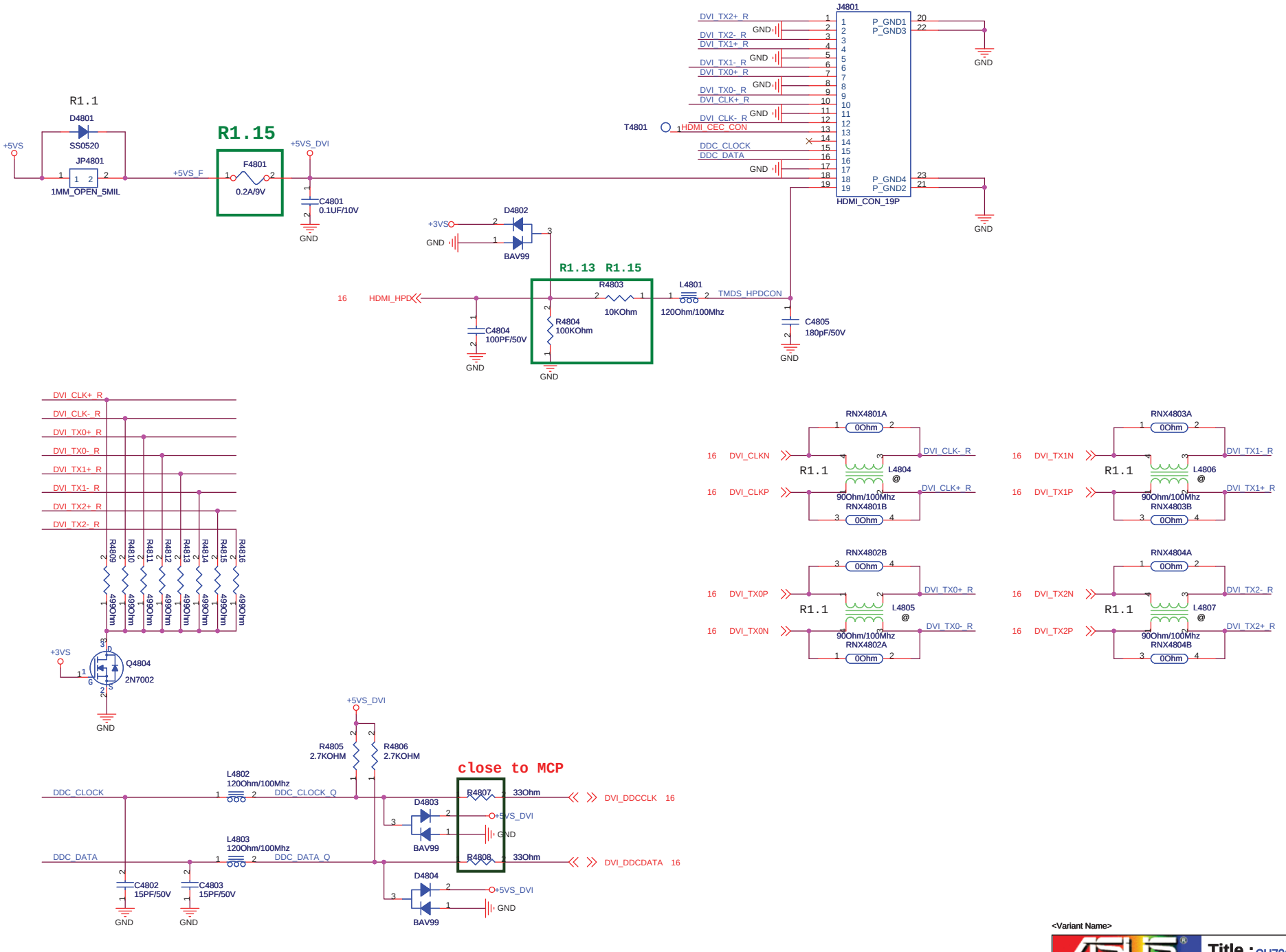
ASUSTeK COMPUTER INC

Title : DDR2 TERM

Engineer:

Size	Project Name	Rev
Custom	1201I	2.0g

Date: Friday, August 28, 2009 Sheet 19 of 54



http://hobi-elektronika.net

<Variant Name>

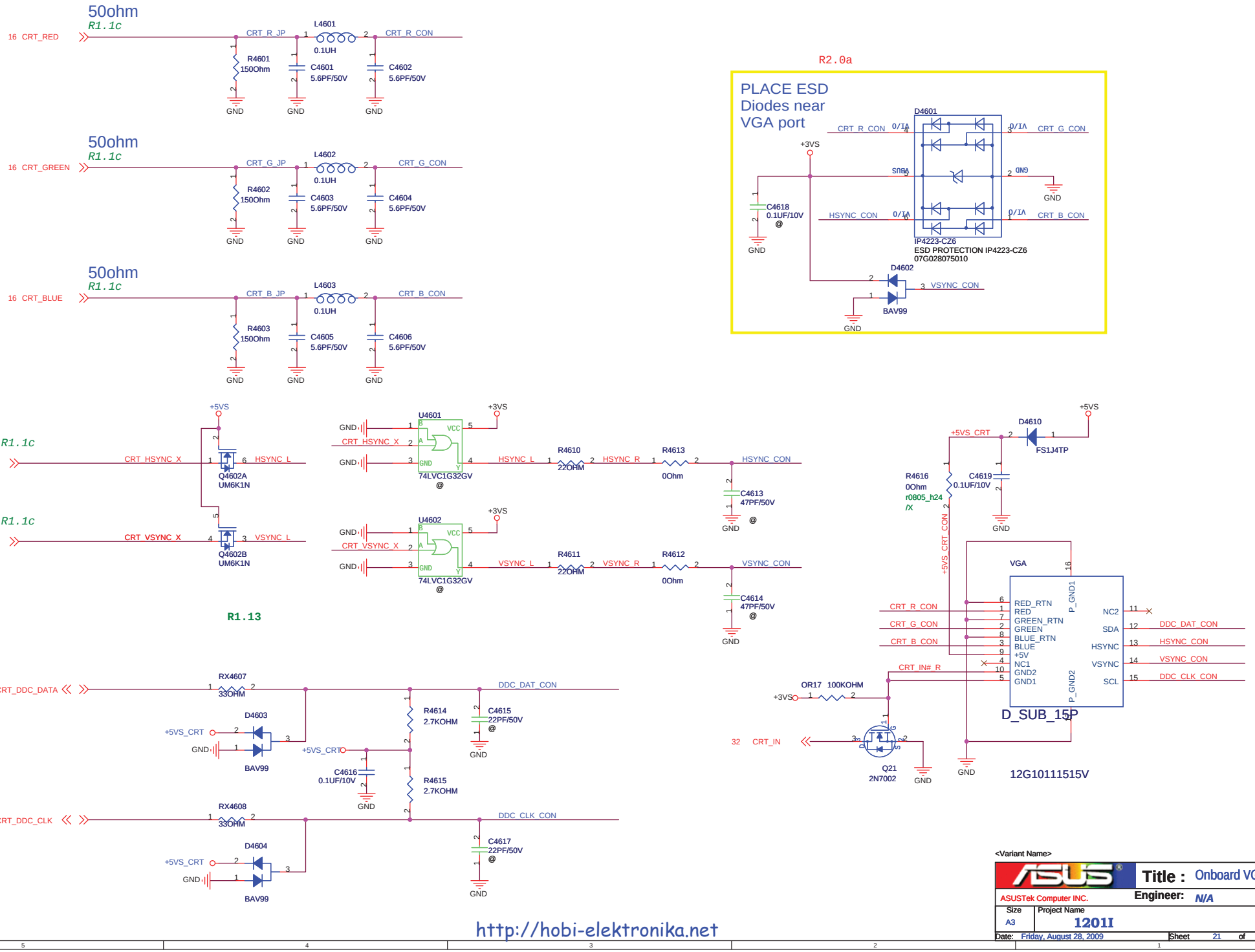
ASUSTek COMPUTER INC

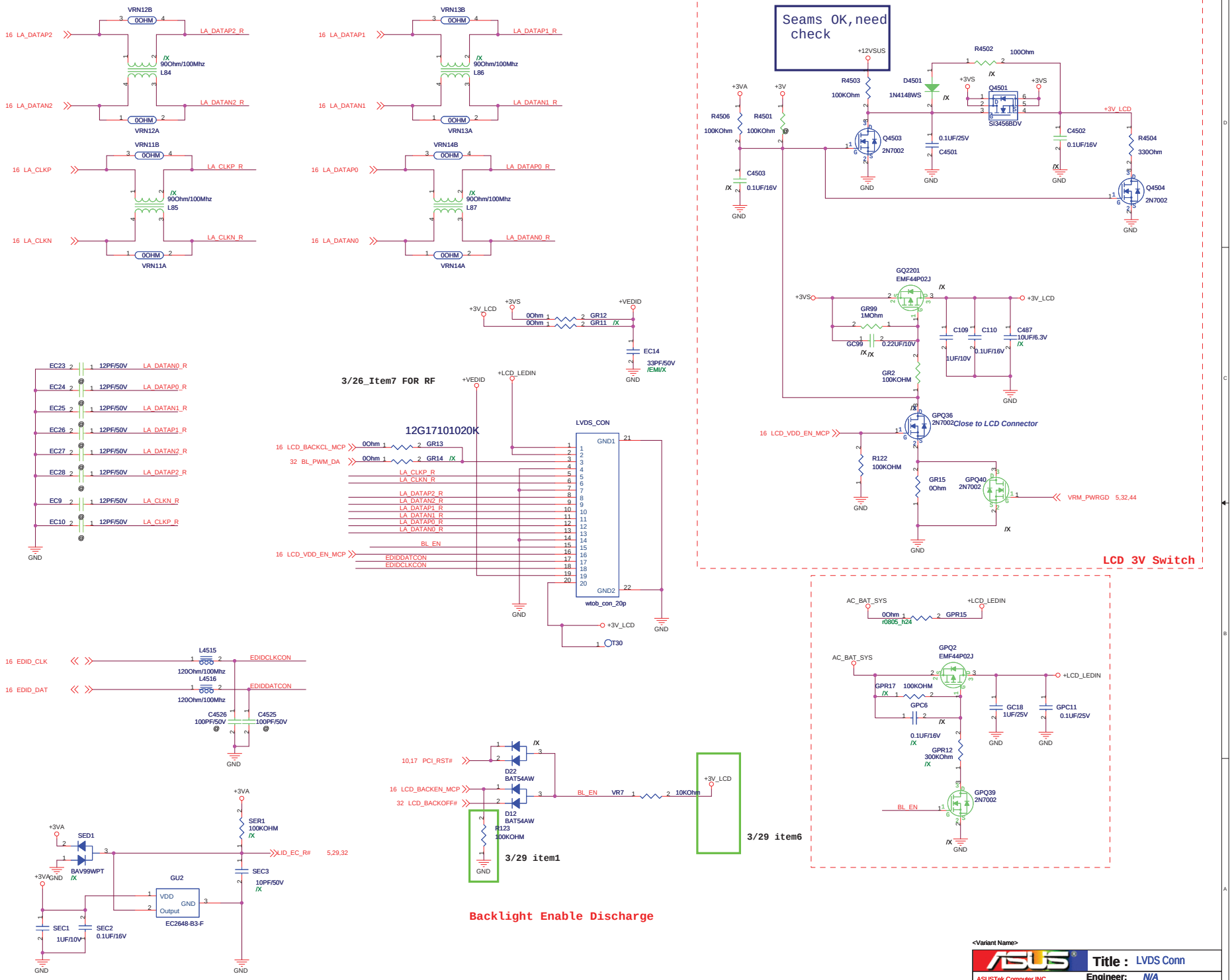
Title : CH7317_SDVO_CRT

Engineer: N/A

Size	Project Name	Rev
A3	1201I	1.0

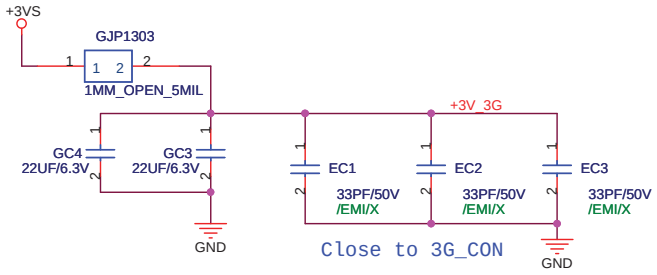
Date: Friday, August 28, 2009 Sheet 20 of 54

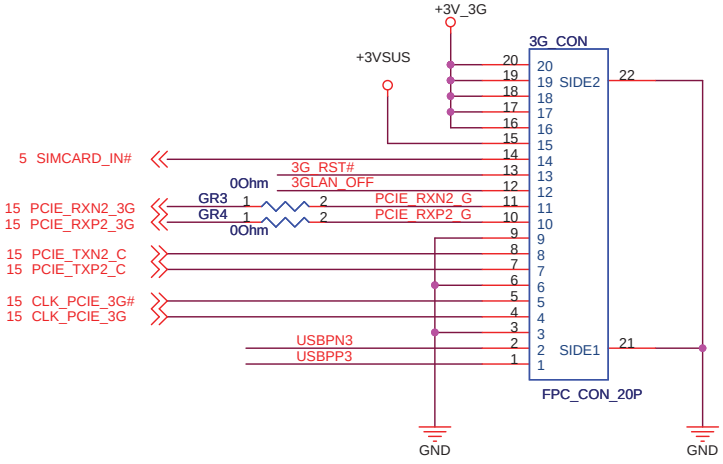

50ohm
R1.1c
16 CRT_RED
CRT_R_JP
L4601
0.1UH
CRT_R_CON
R4601
150Ohm
C4601
5.6PF/50V
C4602
5.6PF/50V
GND
50ohm
R1.1c
16 CRT_GREEN
CRT_G_JP
L4602
0.1UH
CRT_G_CON
R4602
150Ohm
C4603
5.6PF/50V
C4604
5.6PF/50V
50ohm
R1.1c
16 CRT_BLUE
CRT_B_JP
L4603
0.1UH
CRT_B_CON
R4603
150Ohm
C4605
5.6PF/50V
C4606
5.6PF/50V
R2.0a
PLACE ESD
Diodes near
VGA port
D4601
CRT_R_CON
CRT_G_CON
CRT_B_CON
HSYNC_CON
+3VS
C4618
0.1UF/10V
@
IP4223-CZ6
ESD PROTECTION IP4223-CZ6
07G028075010
D4602
VSYNC_CON
BAV99
+5VS
R1.1c
16 CRT_HSYNC
CRT_HSYNC_X
HSYNC_L
Q4602A
UM6K1N
R1.1c
16 CRT_VSYNC
CRT_VSYNC_X
VSYNC_L
Q4602B
UM6K1N
U4601
U4602
74LVC1G32GV
@
R4610
22OHM
R4611
22OHM
R4612
0Ohm
R4613
0Ohm
HSYNC_CON
VSYNC_CON
C4613
47PF/50V
C4614
47PF/50V
R1.13
D4610
FS1J4TP
+5VS_CRT
R4616
0Ohm
r0805_h24
/X
C4619
0.1UF/10V
+5VS_CRT_CON
VGA
RED_RTN
RED
GREEN_RTN
GREEN
BLUE_RTN
BLUE
+5V
NC1
GND2
GND1
P_GND1
P_GND2
NC2
SDA
HSYNC
VSYNC
SCL
DDC_DAT_CON
DDC_CLK_CON
CRT_IN#_R
OR17 100KOHM
32 CRT_IN
Q21
2N7002
D_SUB_15P
12G10111515V
16 CRT_DDC_DATA
RX4607
33OHM
D4603
BAV99
R4614
2.7KOHM
C4615
22PF/50V
@
C4616
0.1UF/10V
R4615
2.7KOHM
16 CRT_DDC_CLK
RX4608
33OHM
D4604
BAV99
C4617
22PF/50V
@
http://hobi-elektronika.net
<Variant Name>
Title : Onboard VGA
ASUSTek Computer INC.
Engineer: N/A
Size A3
Project Name 1201I
Rev 1.0
Date: Friday, August 28, 2009
Sheet 21 of 54

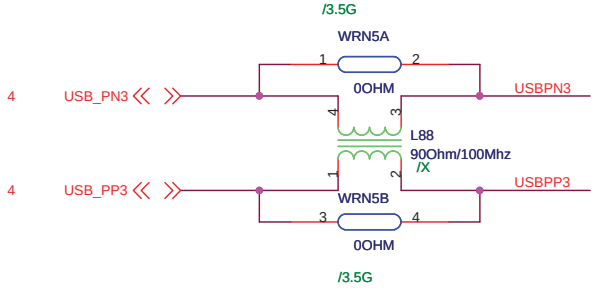


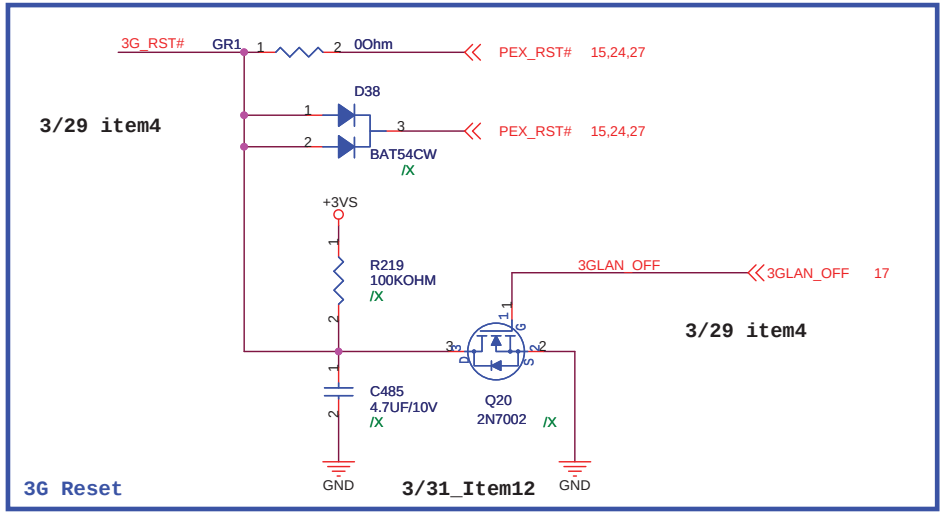
<Variant Name>

Title :	LVDS Conn
ASUSTek Computer INC.	Engineer: N/A
Size: Custom	Project Name: 1201I
Rev: 1.0	
Date: Friday, August 28, 2009	Sheet 22 of 54









<variant_name>
3.5G Module & External Antenna

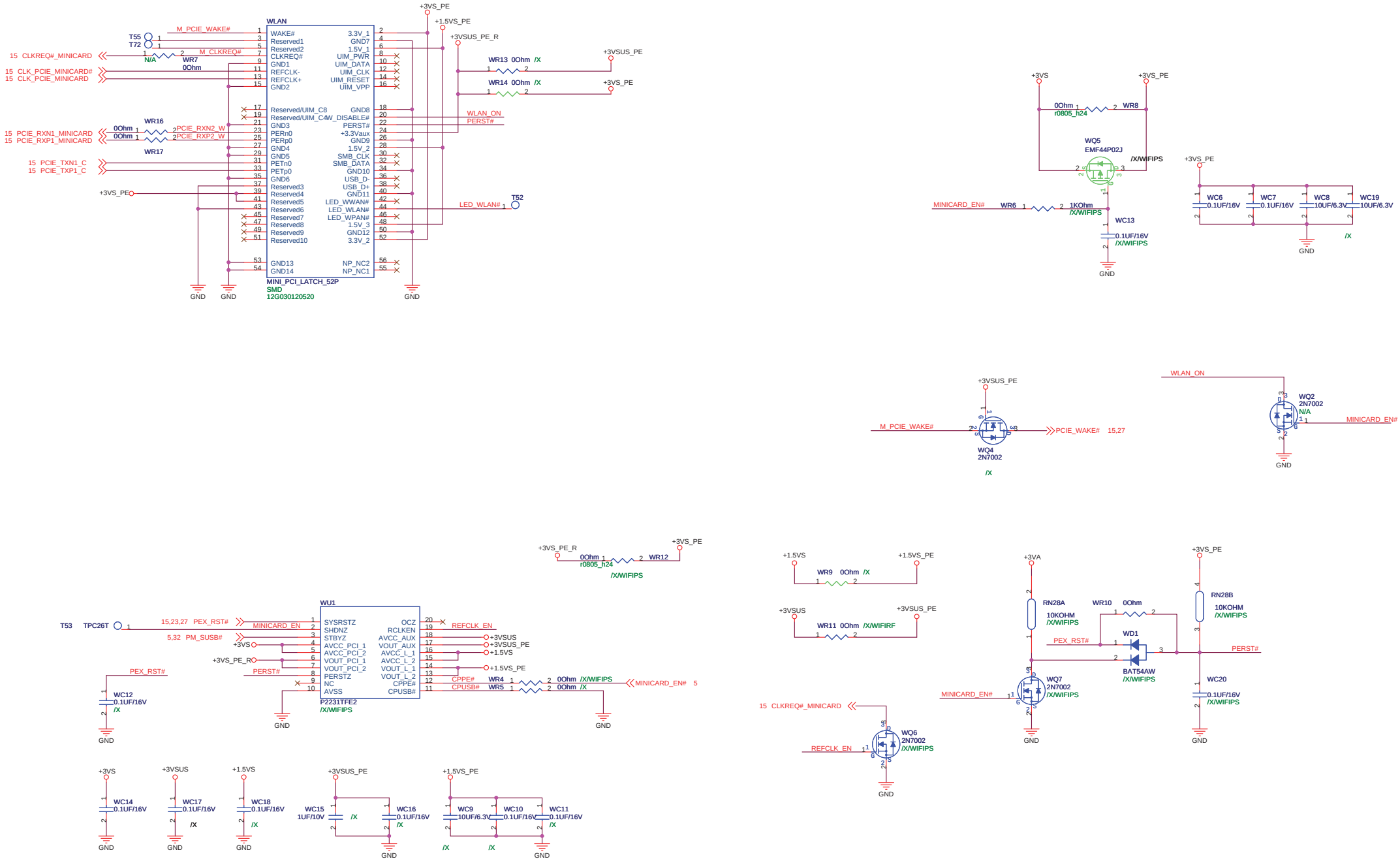
ASUSTek Computer INC.

Title :

Engineer: N/A

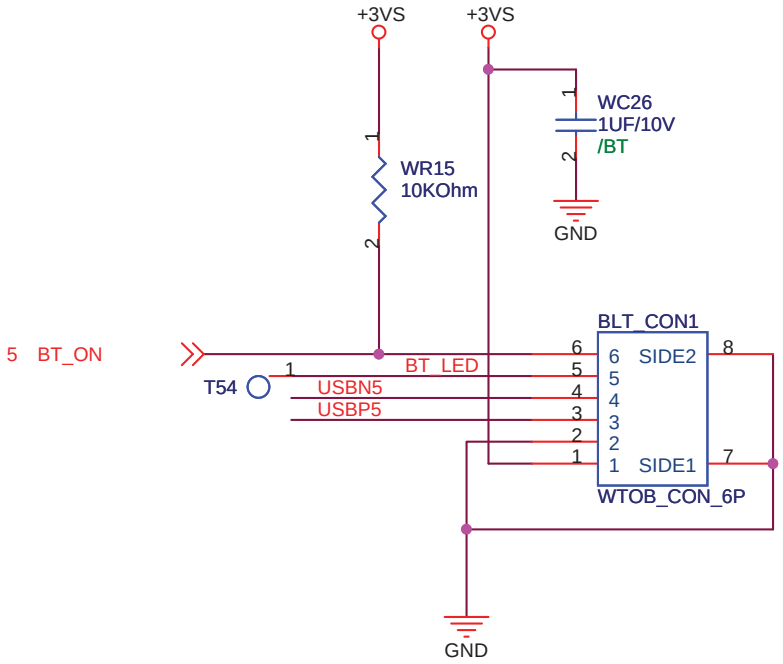
Size	Project Name	Rev
Custom	1201I	1.0

Date: Friday, August 28, 2009 Sheet 23 of 54
</variant_name>

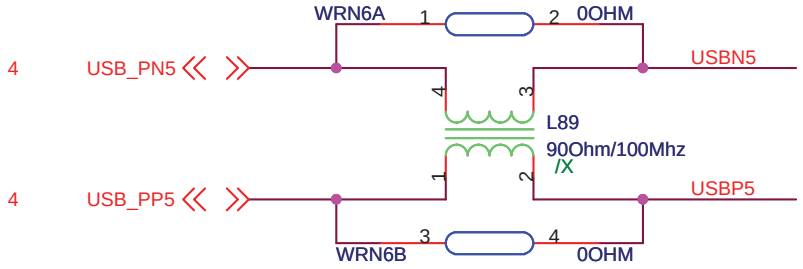


<variant_name>

ASUSTek Computer INC.	Title : Mini WIFI	
	Engineer: N/A	
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 24 of 54	

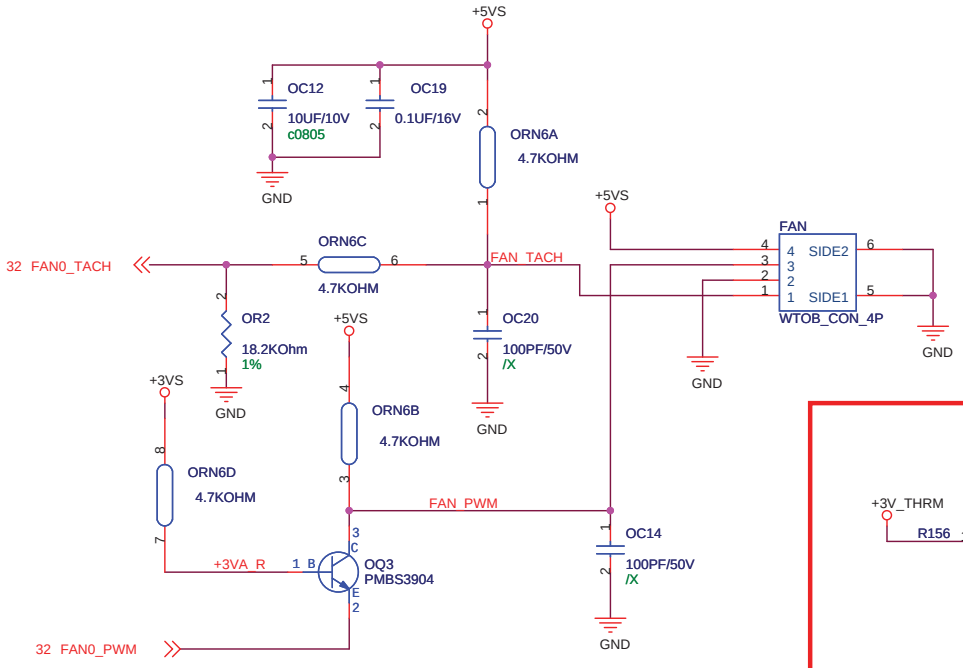


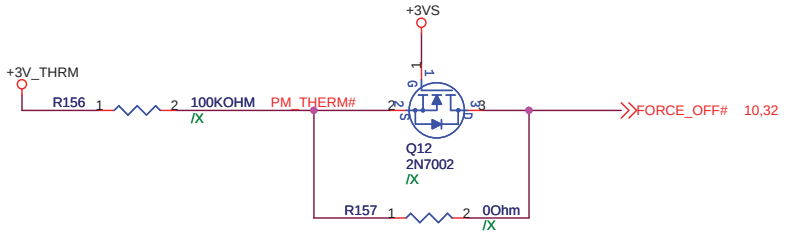
BT Conn

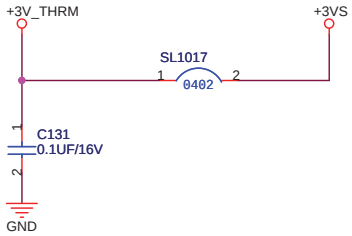


<Variant Name>

ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: N/A	
Size: A	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 25 of 54	

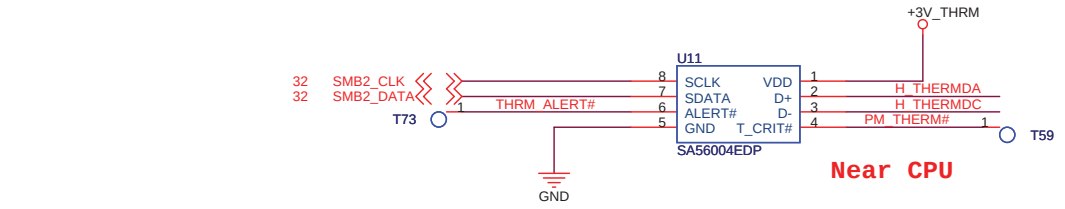






Thermal Sensor Power Supply

Thermal Sensor

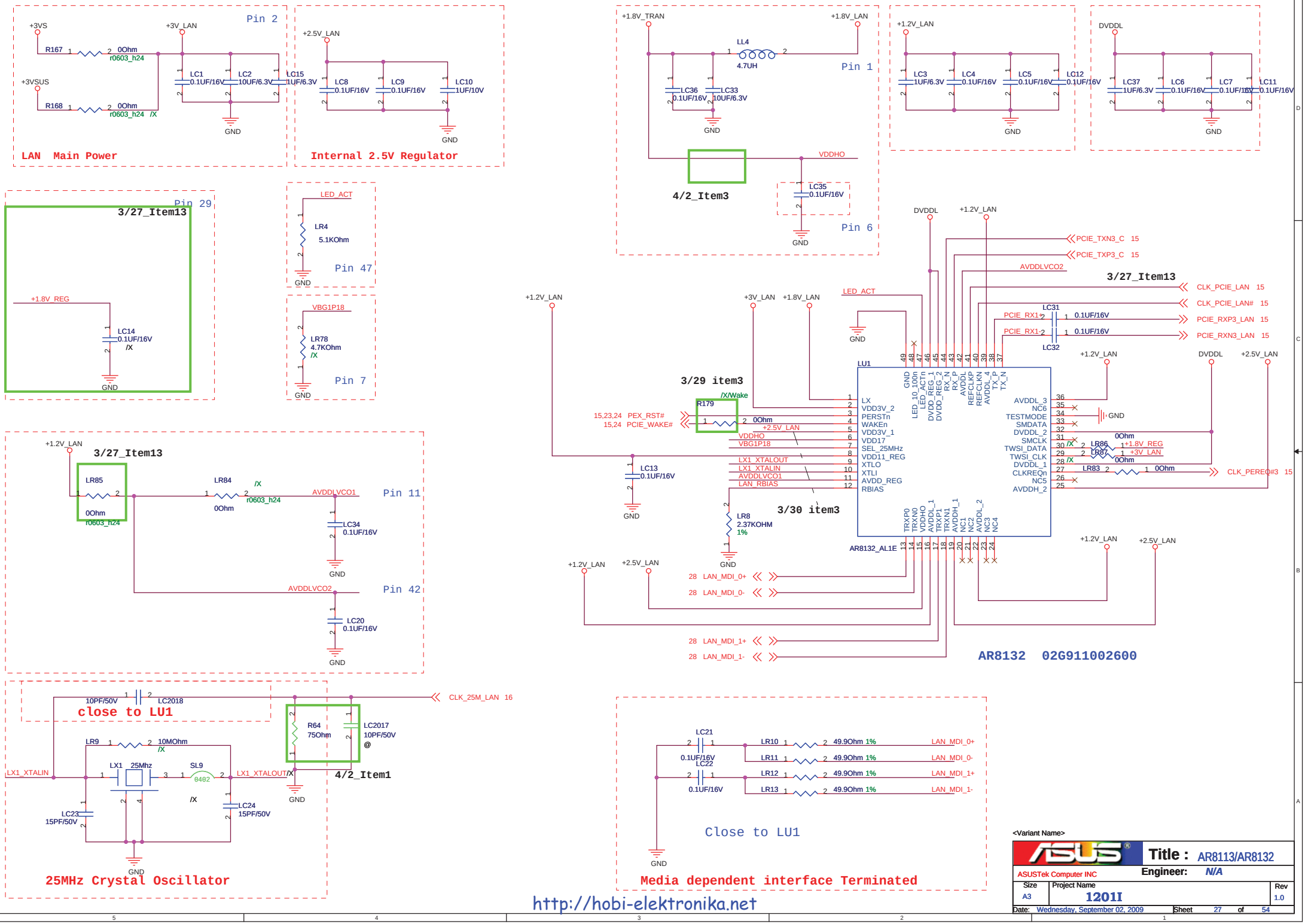


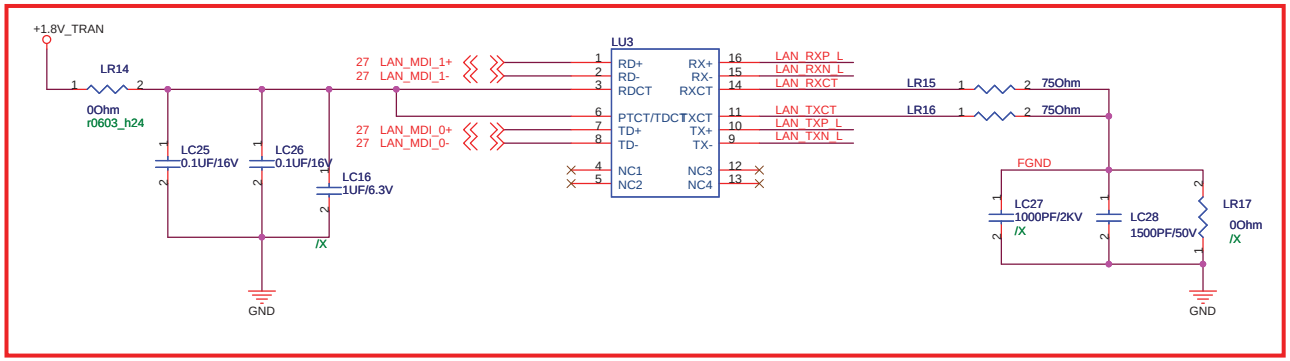
Near CPU

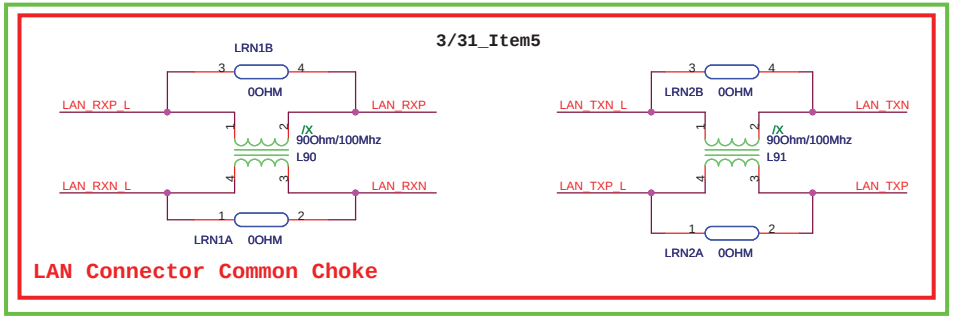
U11 use 06G023044020,
second source 06G023055010

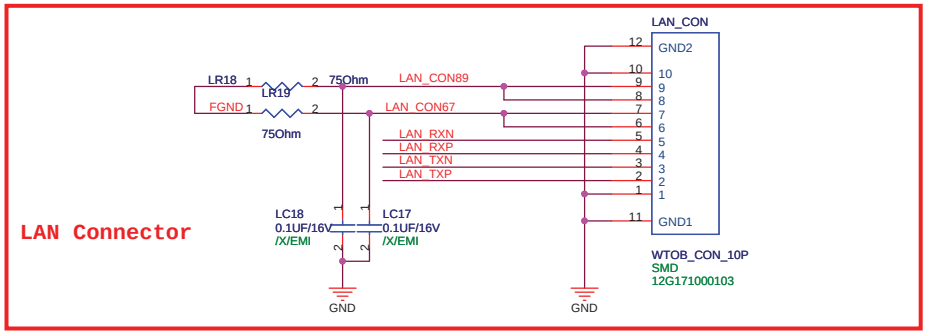
<Variant Name>

ASUSTek Computer INC.	Title : FAN_THERMAL SENSOR	
	Engineer: N/A	
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Wednesday, September 02, 2009	Sheet 26 of 54	









<Variant Name>

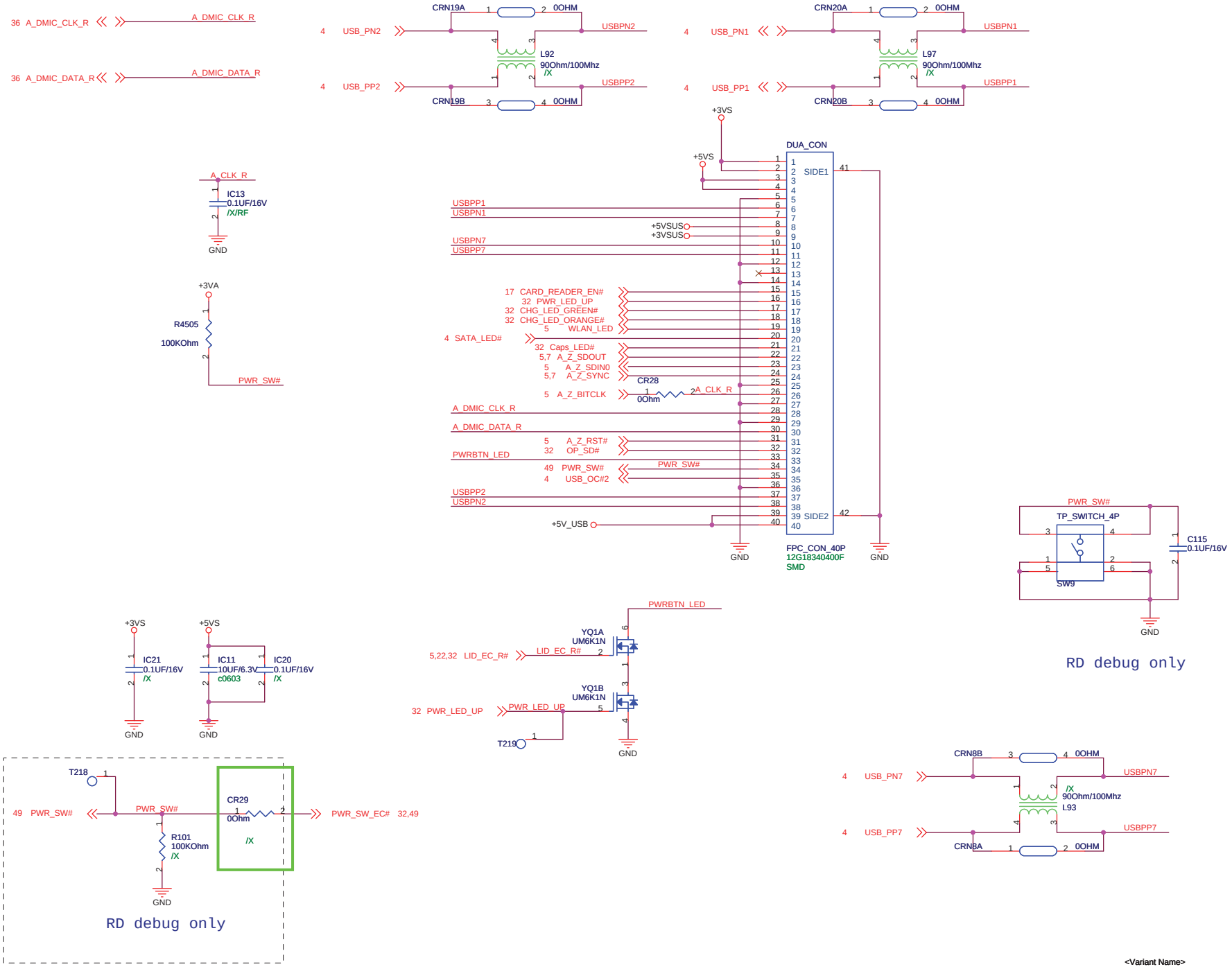
ASUSTek Computer INC.

Title : RJ45

Engineer: N/A

Size	Project Name	Rev
A3	1201I	1.0

Date: Friday, August 28, 2009 Sheet 28 of 54



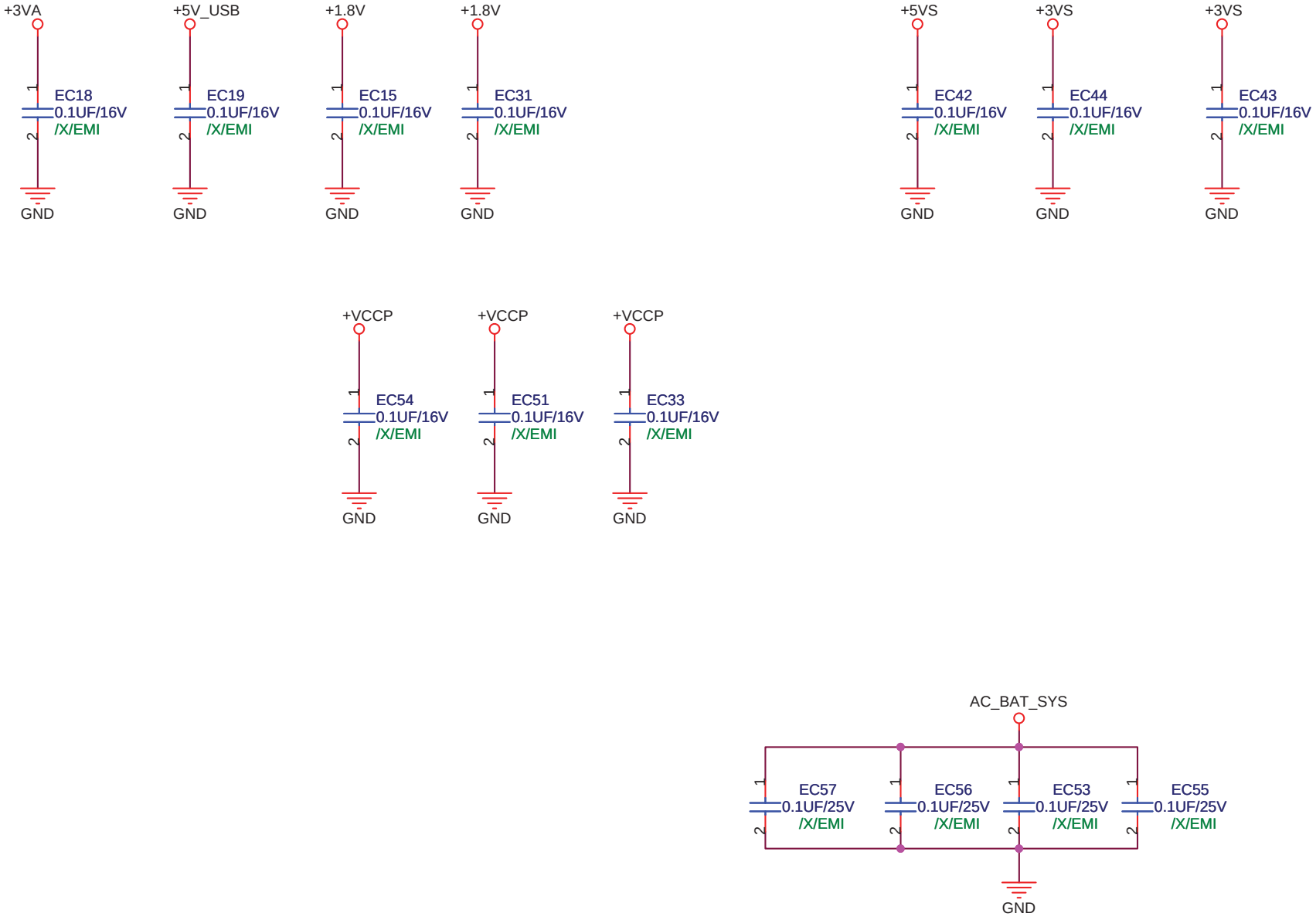
3/26 item11

3/25 item3

http://hobi-elektronika.net

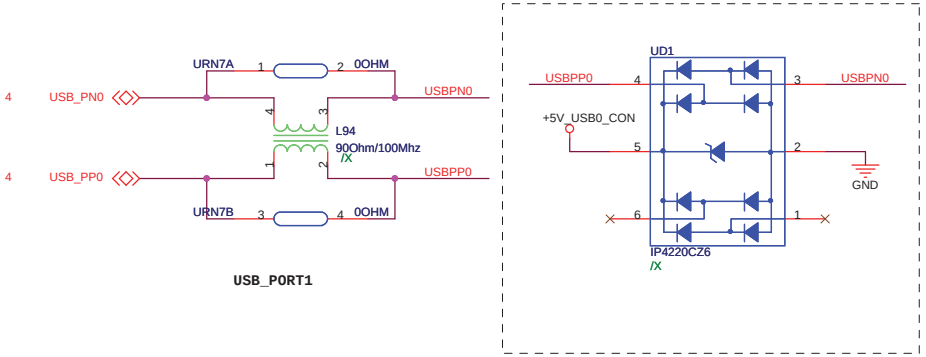
<Variant Name>

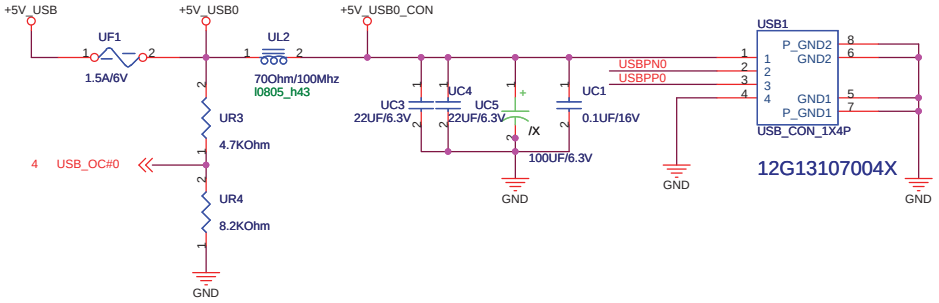
ASUSTek Computer INC.	Title : Flash Conn	
	Engineer: N/A	
Size: A3	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 29 of 54	



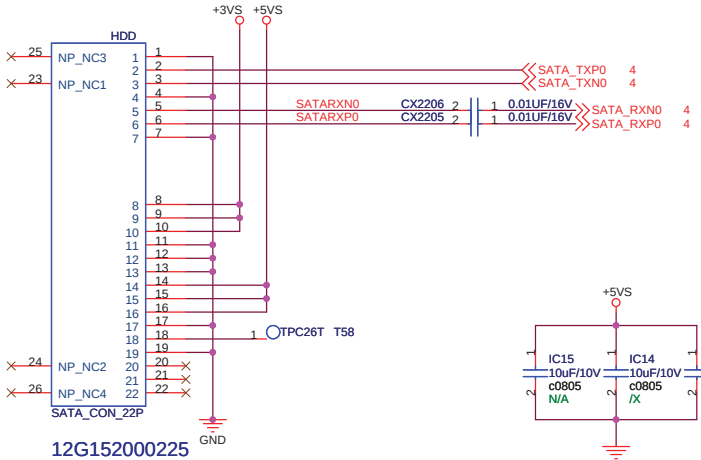
<Variant Name>

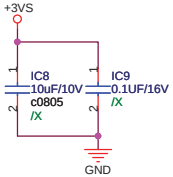
ASUSTek Computer INC.	Title : EMI	
	Engineer: N/A	
Size: A	Project Name: 1201I	Rev: 1.0
Date: Friday, August 07, 2009	Sheet 30 of 54	





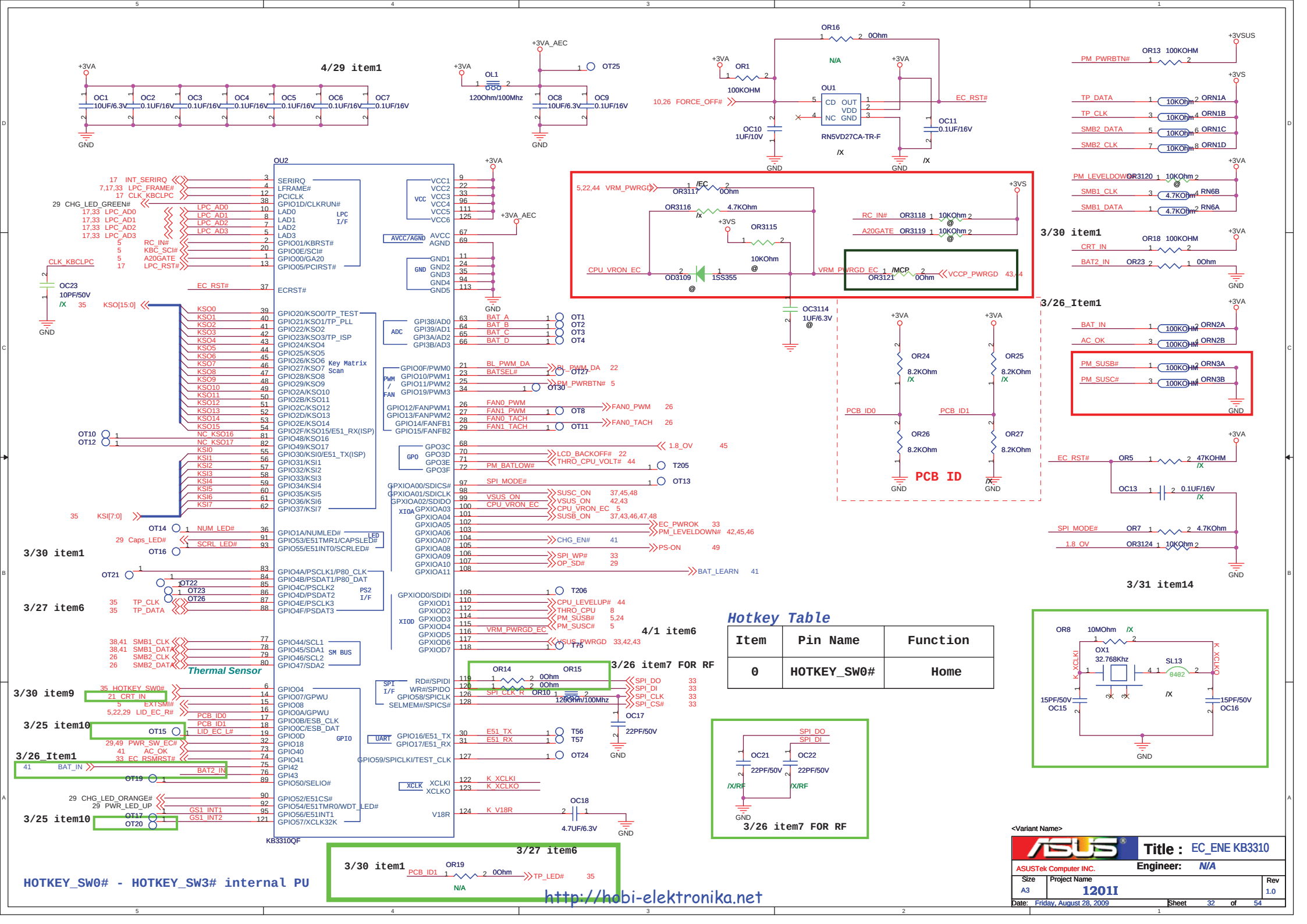
SATA HDD Connector



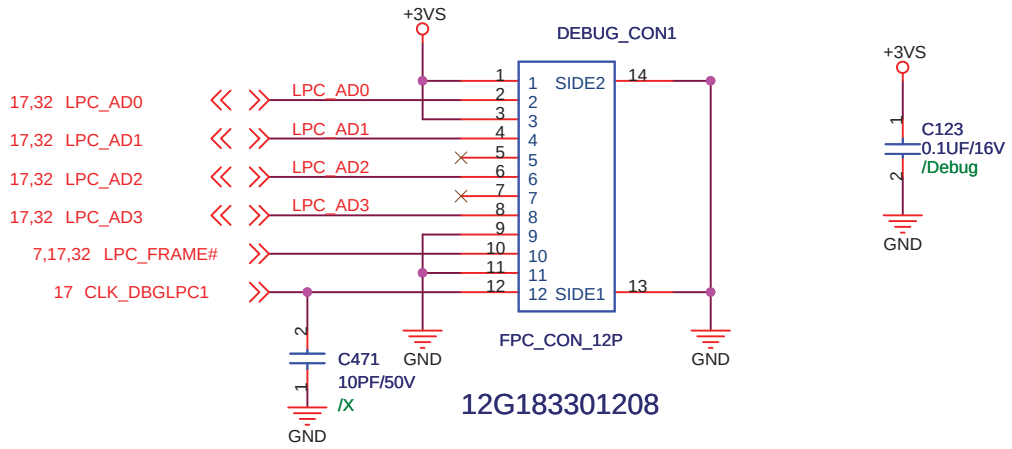


<Variant Name>

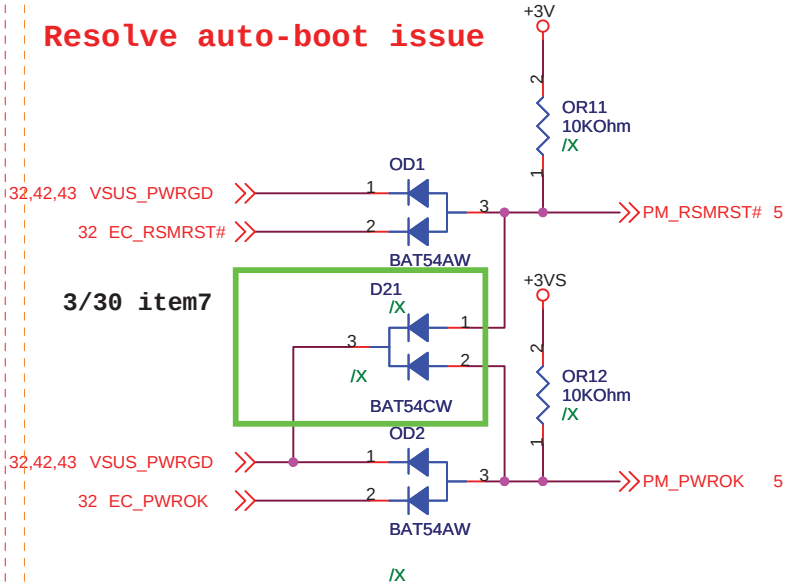
ASUSTek Computer INC.	Title : USB Port	
	Engineer: N/A	
Size: A3	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 31 of 54	


4/29 item1
OU2
KB3310QF
Key Matrix Scan
Thermal Sensor
3/30 item1
3/27 item6
3/30 item9
3/25 item10
3/26_Item1
3/25 item10
4/1 item6
3/26 item7 FOR RF
3/26 item7 FOR RF
3/27 item6
3/30 item1
3/30 item1
3/26_Item1
3/31 item14
PCB ID
Hotkey Table
Item
Pin Name
Function
0
HOTKEY_SW0#
Home
HOTKEY_SW0# - HOTKEY_SW3# internal PU
http://hobi-elektronika.net
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: N/A
Size
A3
Project Name
1201I
Rev
1.0
Date: Friday, August 28, 2009
Sheet 32 of 54

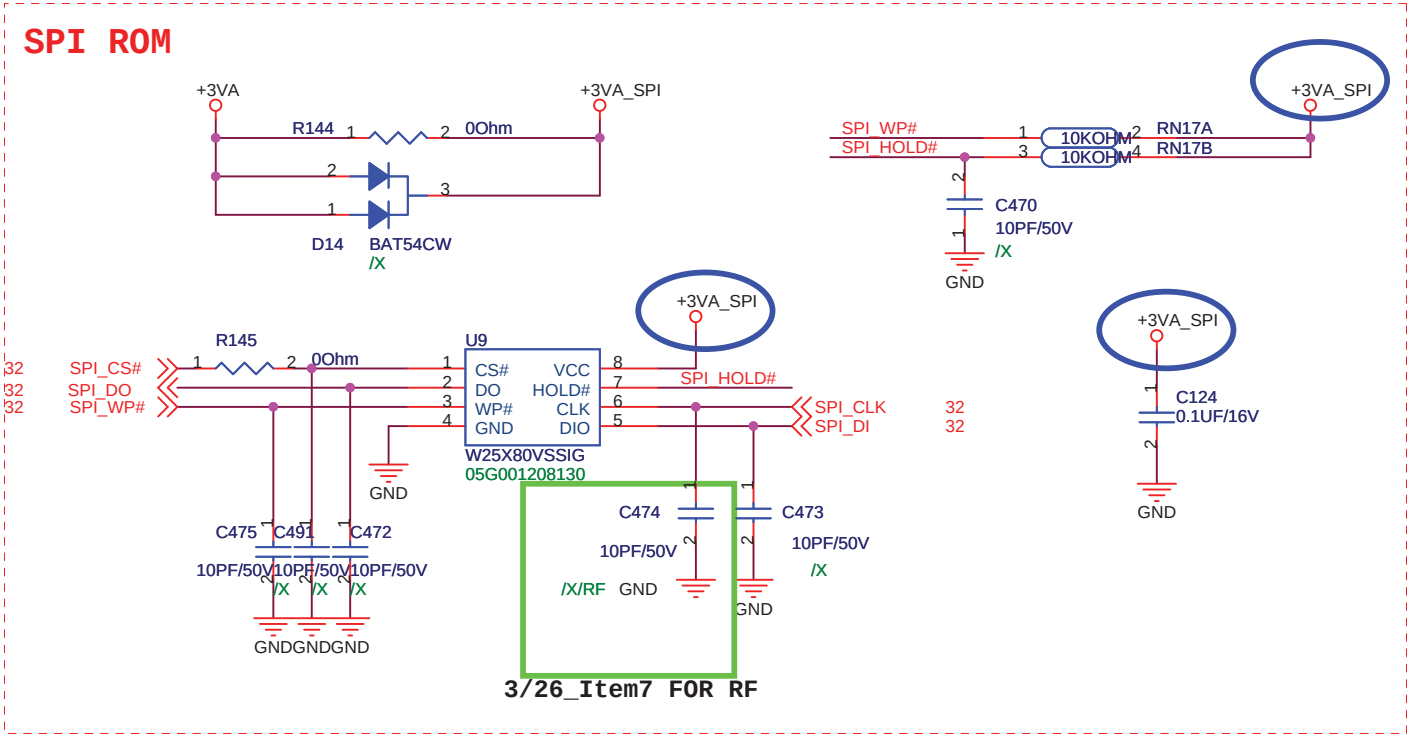
For Debug



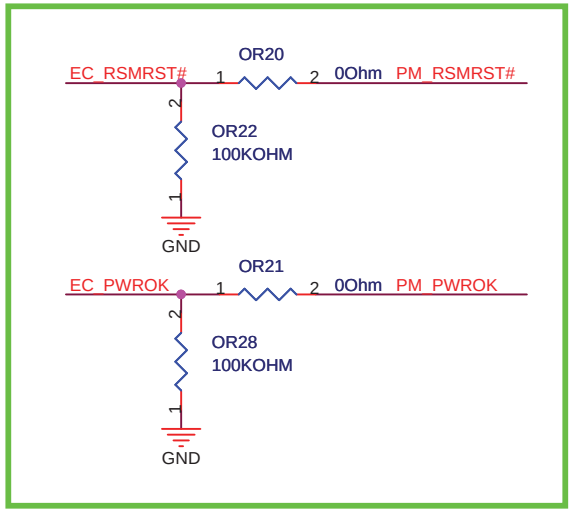
Resolve auto-boot issue



SPI ROM

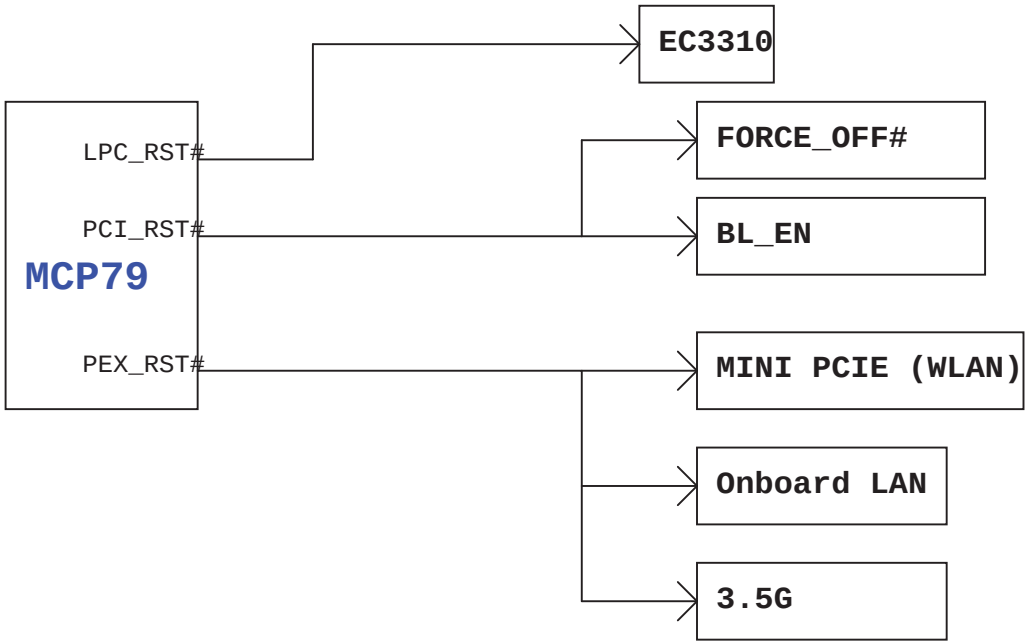


3/30 item7



<Variant Name>

ASUSTek Computer INC.	Title : SPI ROM/ Debug	
	Engineer: N/A	
Size: A4	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 33 of 54	



<Variant Name>

ASUSTeK COMPUTER INC	Title : Reset Map	
	Engineer: N/A	
Size: A4	Project Name: 1201I	Rev: 1.0
Date: Monday, July 20, 2009	Sheet 34 of 54	

For Touch-Pad

12G182102402 pin define

12G182102402

CON2

FPC_CON_24P

KSO[15:0] 32

KSI[7:0] 32

4/3_Item1

D16 D17 D18 D19 D20

PACDN045YB6 /X

3/26_Item7 FOR RF

CN3511A CN3512C CN3511C CN3514C CN3512D CN3512B CN3511D CN3511B CN3516B CN3515D CN3513D CN3515B CN3513A CN3513B CN3514D CN3512A CN3516C CN3516A CN3513C CN3514B CN3514A CN3516D CN3515A CN3515C

33PF/50V /X/RF

For Keyboard Connector

Keyboard ESD Protect

+5VS L26 0Ohm +5V_TP

C196 1UF/10V /X C80 0.1UF/16V

TOUCH_PAD FPC_CON_12P

TP_R TP_L

32 TP_CLK 32 TP_DATA

EC21 33PF/50V /X/EMI EC22 33PF/50V /X/EMI

12G183301208

3/27_Item9

+3VA R203 10KOhm

D3824 BAT54CW /X

HOTKEY_SW0# R HOTKEY_SW0# 32 HOTKEY_SW0#_P 49

0Ohm N/A CB13

TOFFPBTN TP_SWITCH_4P 12G091031041 SMD

EC37 33PF/50V /X

3/27_Item7

R202 10KOhm /X

C153 0.1UF/16V

TP_L TP_R TP_SWITCH_4P SW7 SW8

C112 C111 0.1UF/16V

+5VS TPR2 330Ohm N/A TP_LED BLUE N/A

TP_LED+ TP_LED- TP_LED_G

r0603_h24 TPR3 10KOhm N/A

TPQ1B UM6K1N N/A TPQ1A UM6K1N N/A

32 TP_LED#

EC38 33PF/50V N/A

3/27_Item1

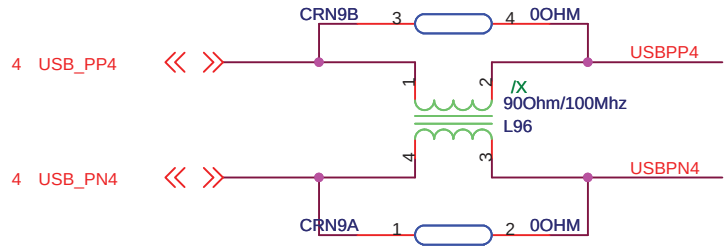
<Variant Name>

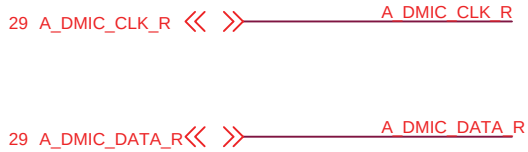
Title : KB_Touch Pad

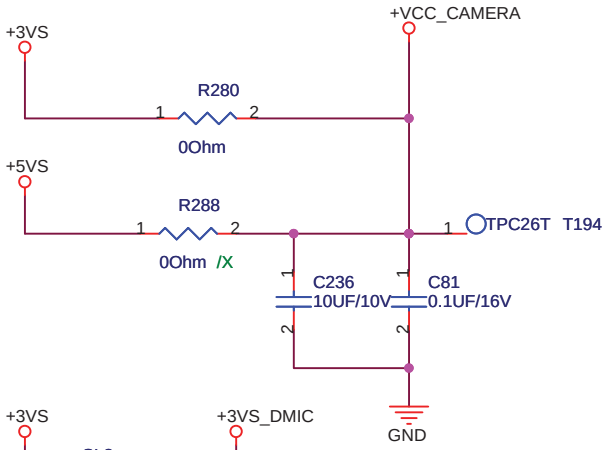
ASUSTek Computer INC. Engineer: N/A

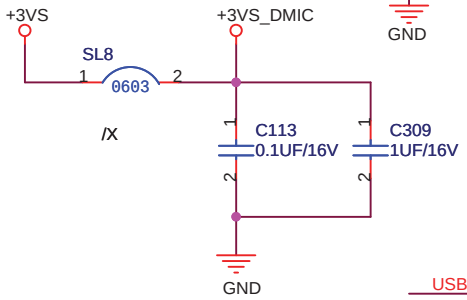
Size	Project Name	Rev
A3	1201I	1.0

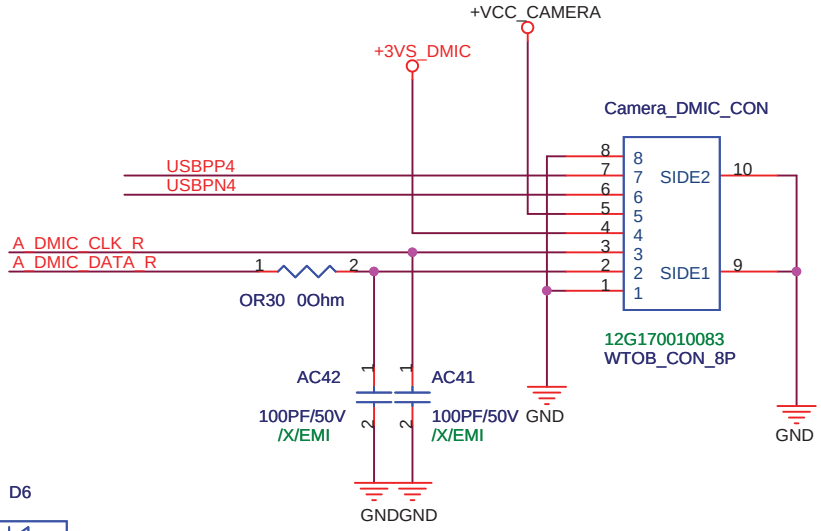
Date: Friday, August 28, 2009 Sheet 35 of 54

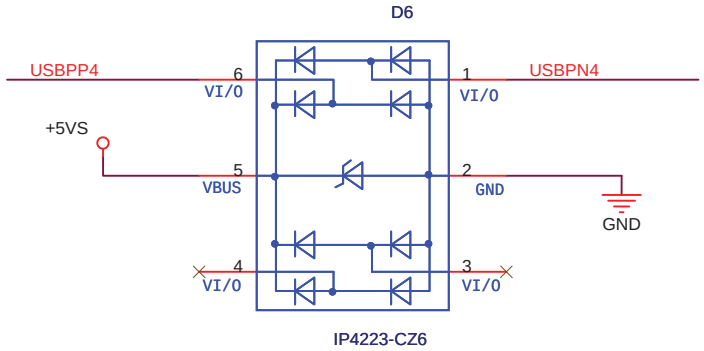






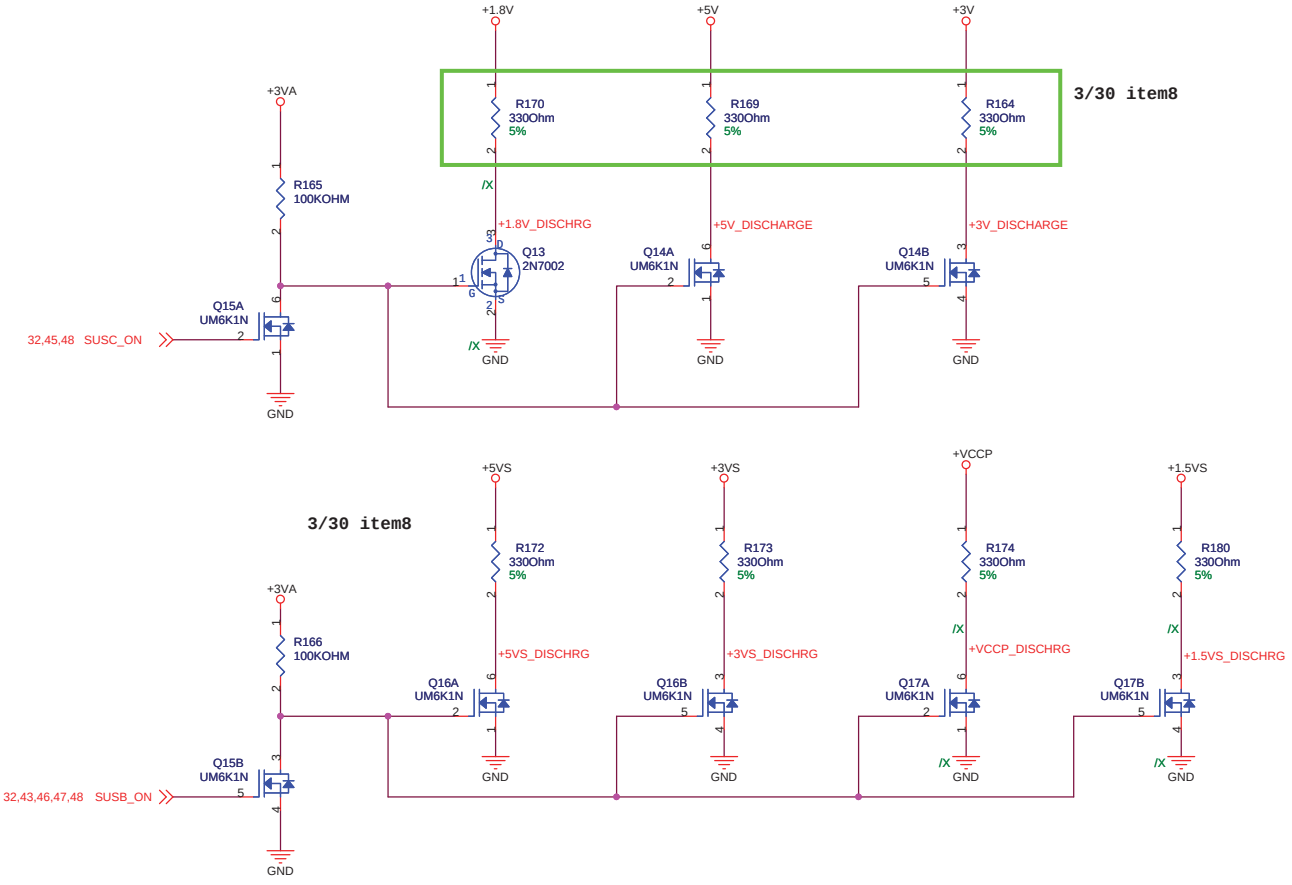






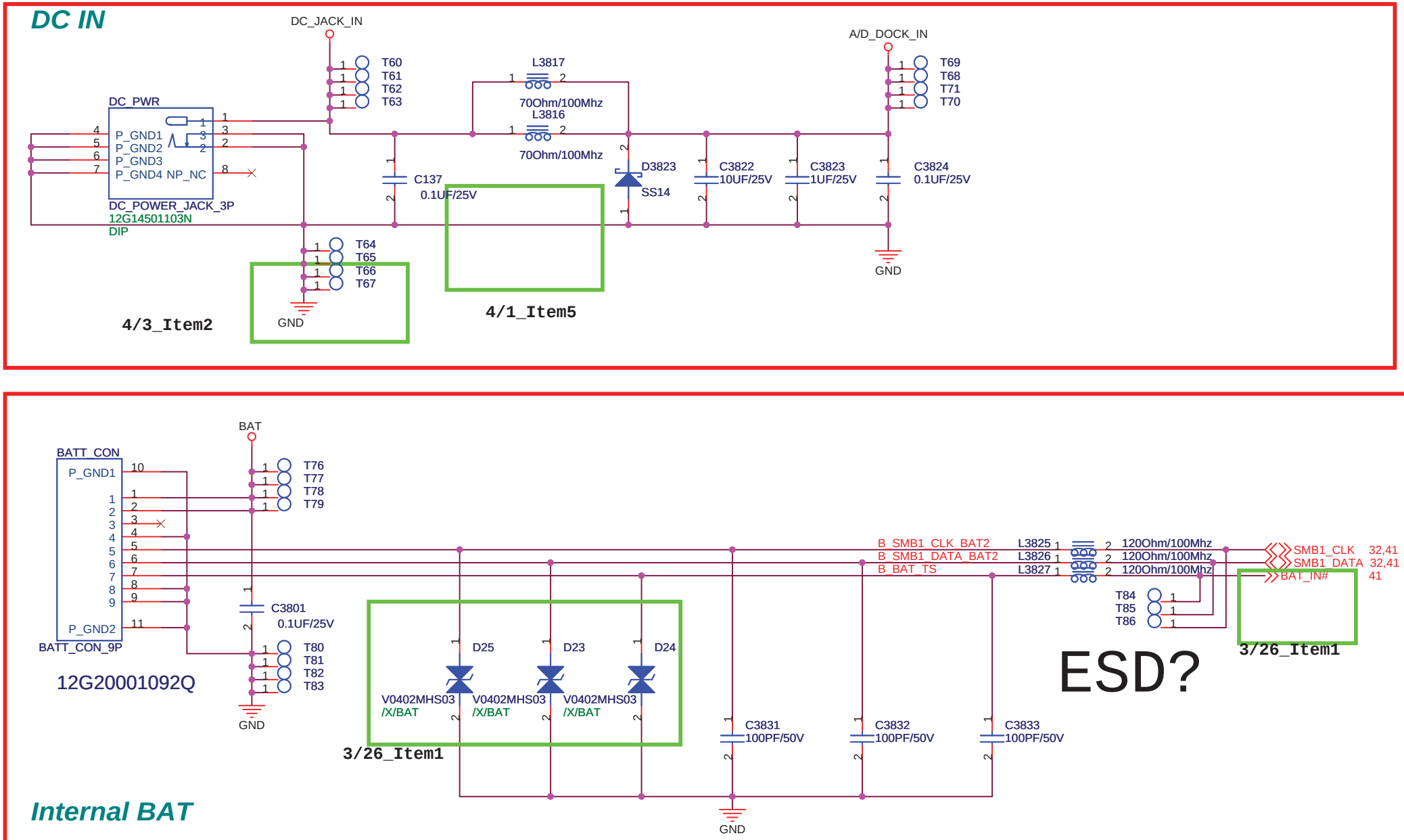
<Variant Name>

ASUSTek Computer INC.	Title : CMOS	
	Engineer: N/A	
Size: A4	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 36 of 54	



<Variant Name>

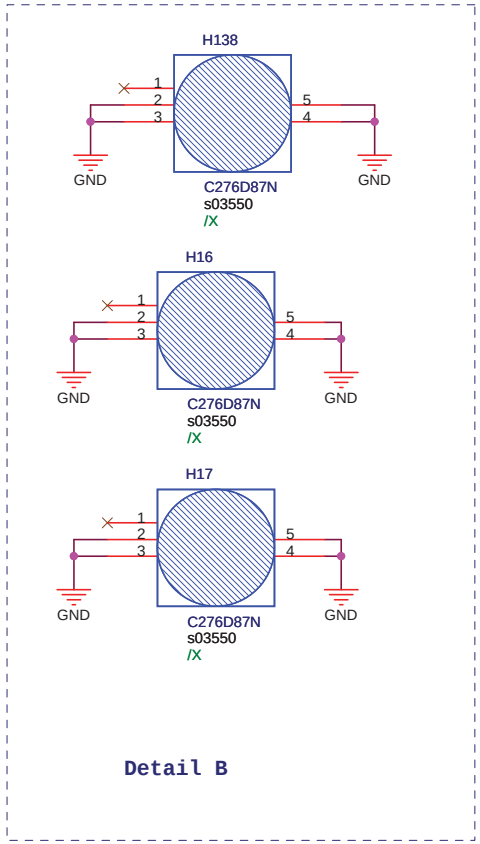
ASUSTek Computer INC.	Title : Discharge	
	Engineer: N/A	
Size: A3	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 37 of 54	

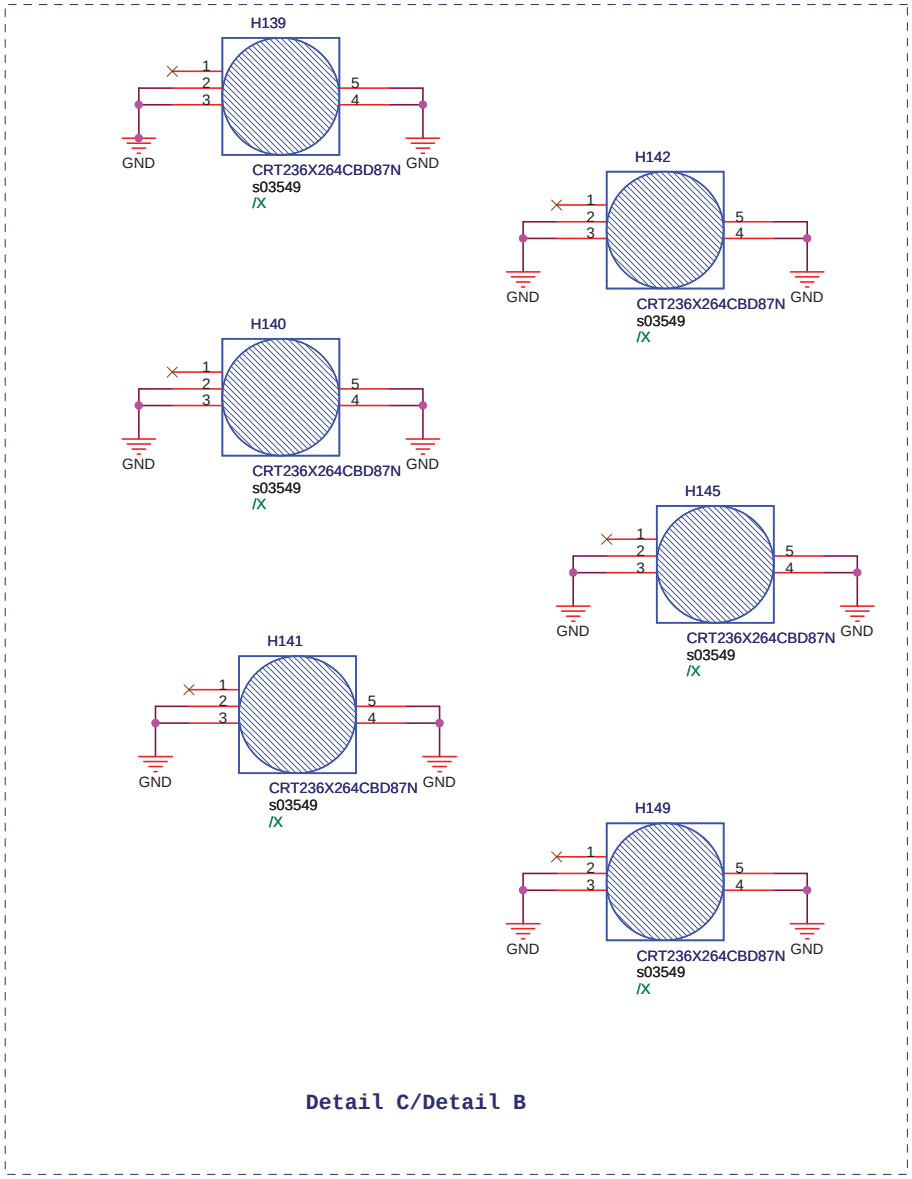


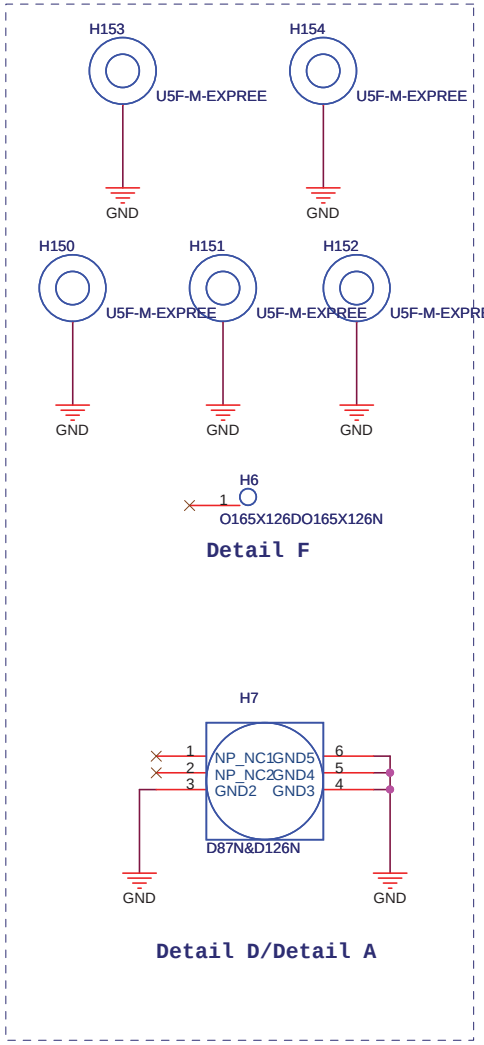
http://hobi-elektronika.net

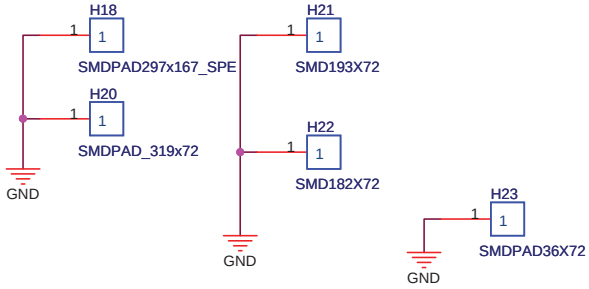
<Variant Name>

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: N/A	
Size: A4	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 38 of 54	









<variant_name>

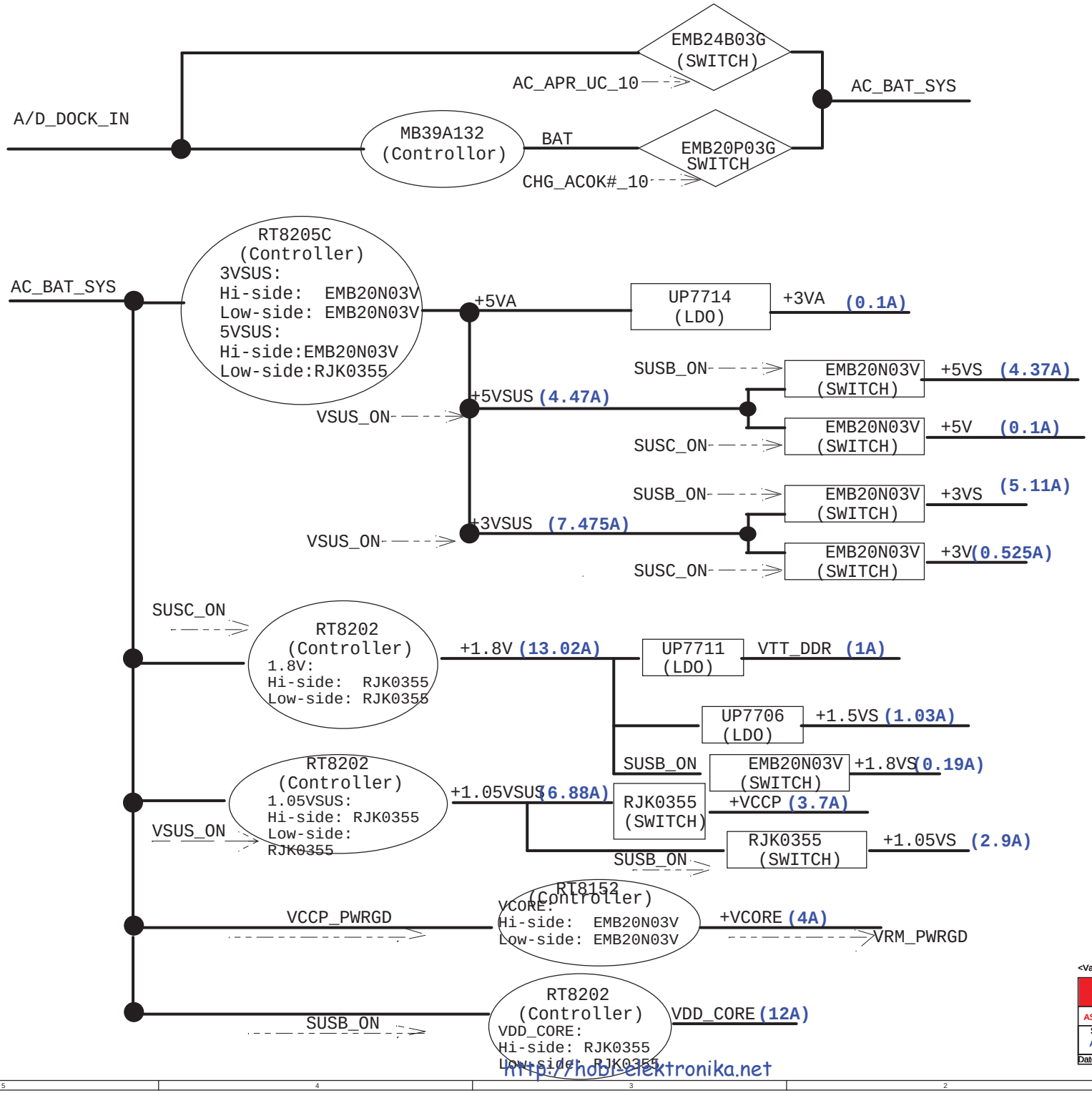
ASUSTek Computer INC.

Title : Screw Hole

Engineer: N/A

Size	Project Name	Rev
Custom	1201I	1.0

Date: Thursday, September 03, 2009 Sheet 39 of 54



<Variant Name>

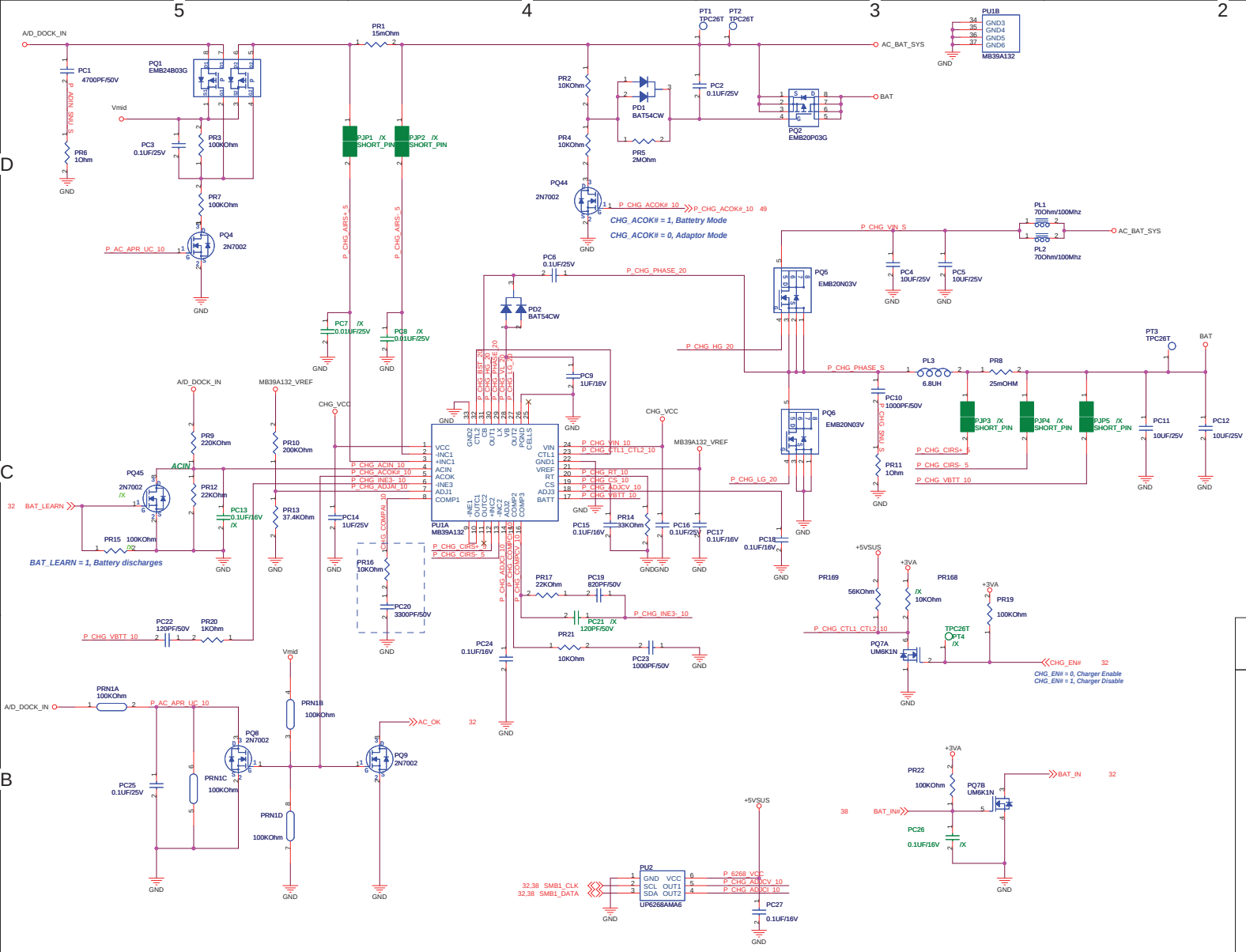
Title : Power Flow

ASUSTek Computer INC.

Engineer: Jerry Liu

Size	Project Name	Rev
A3	1201i	1.2

Date: Wednesday, August 26, 2009 Sheet 40 of 54



Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.64A
2. Ripple Current:
   I ripple =0.875A
   I spec=2A ⊙1 pcs
3. Inductor Spec:
   I sat=8 A
   I dc =4.5A
   DCR=60mohm
4. MOSFET Spec:

H-side MOSFET:EMB20N03V

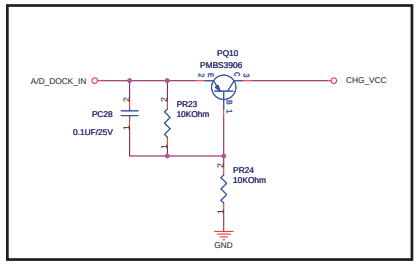
Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

L-side MOSFET: EMB20N03V

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:
   +12.6V@2.5A
2. Frequency:
   PR122=33KOHM,
   Fosc=17000/RT(Kohm)=515KHz
3. OCP:
4. POR:
   POR Hysteresis =0.1V
   V on =7.5V
5. Enable Voltage:
   V = 2.9 V
6. Soft start time:
   Tss=23ms
7. Phase selection:
   N/A
8. Inrush Current:
   C total =20uF
   I inrush= 0.01A



Battery Charging Current :

Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

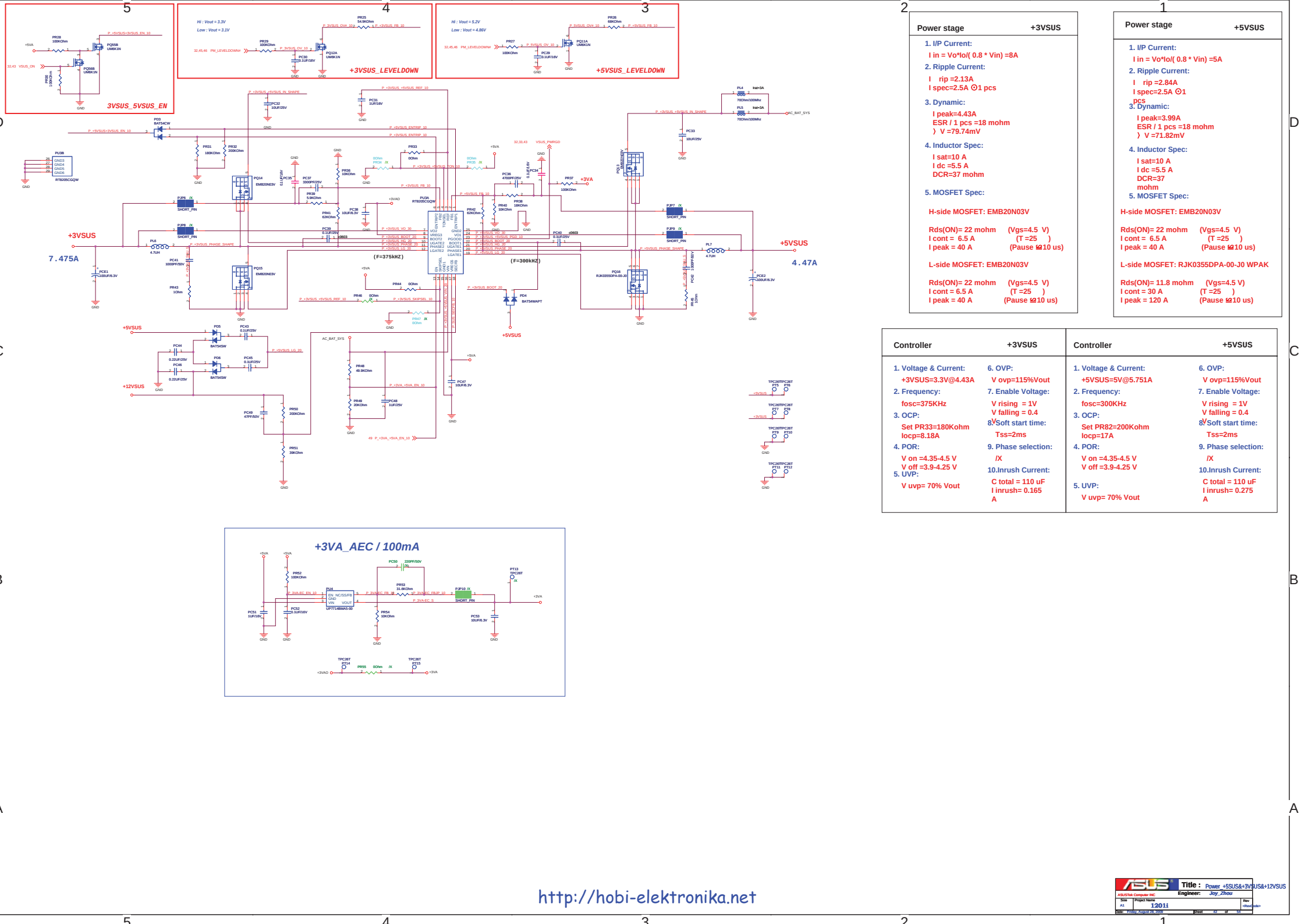
CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.23 * CS (uF)*

Title : Charger			
ASUSTek Computer INC	Engineer: Joy_Zhou		
Size: A2	Project Name: 12011		Rev: <RevCode>
Date: Friday, August 28, 2009	Sheet 41 of 54		

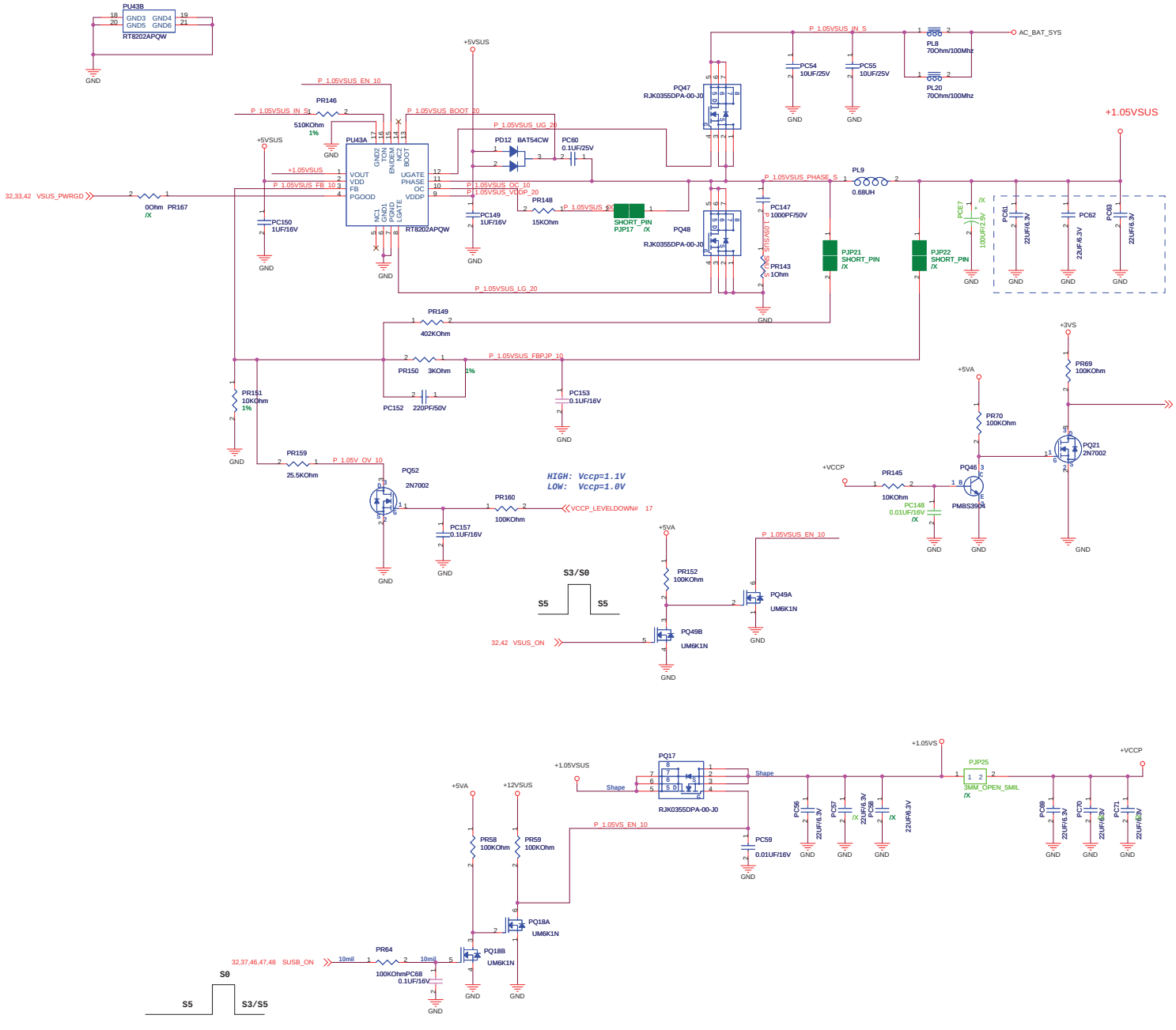


Power stage	+3VSUS
1. I/P Current:	I in = Vo*Io/(0.8 * Vin) =8A
2. Ripple Current:	I rip =2.13A I spec=2.5A ⊙1 pcs
3. Dynamic:	I peak=4.43A ESR / 1 pcs =18 mohm 〉V =79.74mV
4. Inductor Spec:	I sat=10 A I dc =5.5 A DCR=37 mohm
5. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 22 mohm	(Vgs=4.5 V)
I cont = 6.5 A	(T =25)
I peak = 40 A	(Pause ≦10 us)
L-side MOSFET: EMB20N03V	
Rds(ON)= 22 mohm	(Vgs=4.5 V)
I cont = 6.5 A	(T =25)
I peak = 40 A	(Pause ≦10 us)

Power stage	+5VSUS
1. I/P Current:	I in = Vo*Io/(0.8 * Vin) =5A
2. Ripple Current:	I rip =2.84A I spec=2.5A ⊙1 pcs
3. Dynamic:	I peak=3.99A ESR / 1 pcs =18 mohm 〉V =71.82mV
4. Inductor Spec:	I sat=10 A I dc =5.5 A DCR=37 mohm
5. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 22 mohm	(Vgs=4.5 V)
I cont = 6.5 A	(T =25)
I peak = 40 A	(Pause ≦10 us)
L-side MOSFET: RJK0355DPA-00-J0 WPAK	
Rds(ON)= 11.8 mohm	(Vgs=4.5 V)
I cont = 30 A	(T =25)
I peak = 120 A	(Pause ≦10 us)

Controller	+3VSUS	Controller	+5VSUS
1. Voltage & Current:	+3VSUS=3.3V@4.43A	1. Voltage & Current:	+5VSUS=5V@5.751A
2. Frequency:	fosc=375KHz	2. Frequency:	fosc=300KHz
3. OCP:	Set PR33=180Kohm Iocp=8.18A	3. OCP:	Set PR82=200Kohm Iocp=17A
4. POR:	V on =4.35-4.5 V V off =3.9-4.25 V	4. POR:	V on =4.35-4.5 V V off =3.9-4.25 V
5. UVP:	V uvp= 70% Vout	5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout	6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4	7. Enable Voltage:	V rising = 1V V falling = 0.4
8. Soft start time:	Tss=2ms	8. Soft start time:	Tss=2ms
9. Phase selection:	/X	9. Phase selection:	/X
10.Inrush Current:	C total = 110 uF I inrush= 0.165 A	10.Inrush Current:	C total = 110 uF I inrush= 0.275 A

Title :	Power_+5SUS&+3VSUS&+12VSUS
Engineer:	Joy_Zhou
Size	A1
Project Name	12011
Rev	<RevCode>
Date:	Friday, August 24, 2012
Sheet	42 of 54



Power stage

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =1.7A

2. Ripple Current:

I rip =2.72A
I spec=2.5A
⊙2pcs

3. Dynamic:

I peak=2.5A
ESR / 1 pcs =18 mohm
〉V =45mV

4. Inductor Spec:

I SAC=25.5A
IDC =15.5 A
DCR=5mohm

5. MOSFET Spec:

H-side MOSFET:RJK0355DPA-00-J0

Rds(ON)= 16.5mOhm (Vgs=4.5 V)
I cont = 30 A (T =25)
I peak =120 A (Pause ≦10 us)

L-side MOSFET: RJK0355DPA-00-J0

Rds(ON)= 16.5mOhm (Vgs=4.5 V)
I cont =30 A (T =25)
I peak =120 A (Pause ≦10 us)

Controller

1. Voltage & Current:

+1.05V@6.88A

2. Frequency:

PR146=510K ohm
Fosc=480KHz

3. OCP:

PR148=15K ohm -> 18A

4. POR:

Vccrth =3.7~4.1V
Vcchys=0.2V

5. UVP:

Vout*70%

6. OVP:

Vout*115%

7. Enable Voltage:

V = 2.9V

8. Soft start time:

Tss=1.2 ms

9. Phase selection:

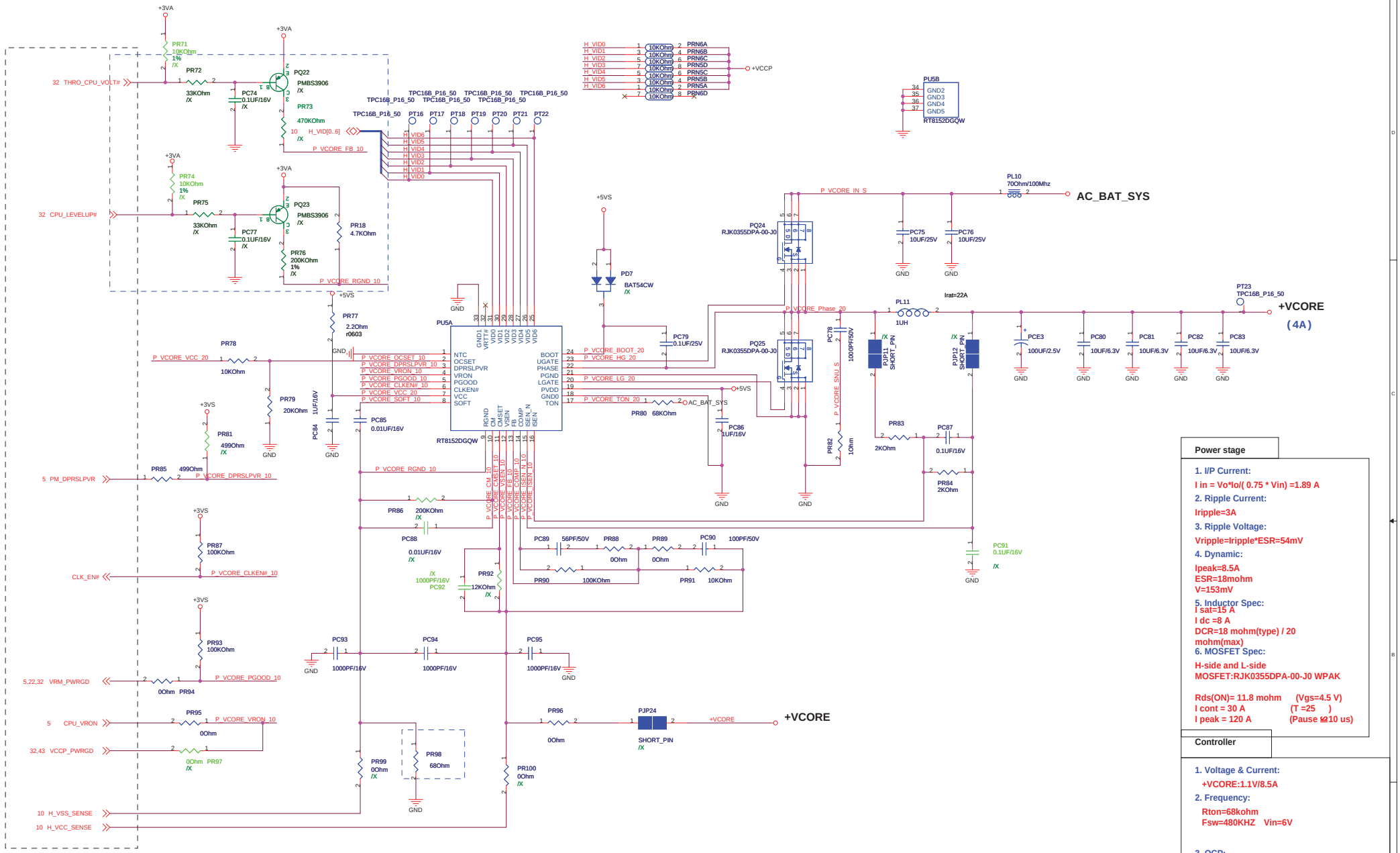
/X

10.Inrush Current:

C total = 100 uF
I inrush= 0.15 A

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_1.05v	
	Engineer: Joy_zhou	
Size: A2	Project Name: 12011	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 43 of 54	



THRO_CPU_VOLT#	CPU_LEVELUP#	Voltage	Status
L	H	VID-50mV	Power Saving
H	H	VID	Normal
H	L	VID+50mV	Performance

Power stage

1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =1.89 A
2. Ripple Current:
Iripple=3A
3. Ripple Voltage:
Vripple=Iripple*ESR=54mV
4. Dynamic:
Ipeak=8.5A
ESR=18mohm
V=153mV
5. Inductor Spec:
I sat=15 A
I dc =8 A
DCR=18 mohm(type) / 20 mohm(max)
6. MOSFET Spec:
H-side and L-side
MOSFET:RJK0355DPA-00-J0 WPAK

Rds(ON)= 11.8 mohm (Vgs=4.5 V)
I cont = 30 A (T =25)
I peak = 120 A (Pause ≦10 us)

Controller

1. Voltage & Current:
+VCORE:1.1V/8.5A
2. Frequency:
Rton=68kohm
Fsw=480KHZ Vin=6V

3. OCP:
DCR*Imax*PR235/(PR232+PR235)=83.3mV
Imax=16.6A
4. On time:
Ton=265~580ns
5.LoadLine:
Rcs=PR84/(PR83+PR84)*Rdcr
=5mohm

<Variant Name>

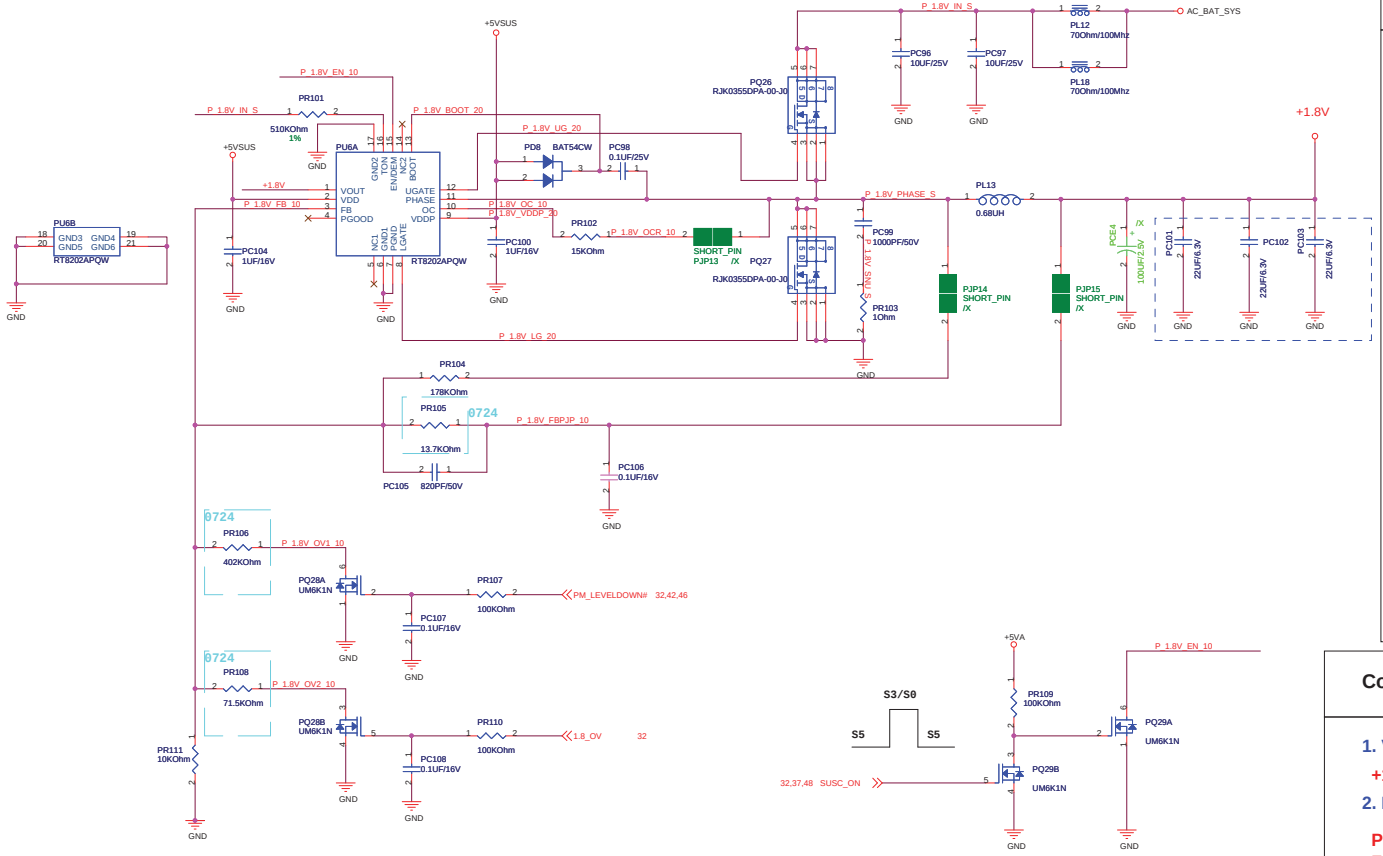
ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE_RT8152

Engineer: Joy_zhou

Size	Project Name	Rev
C	1201i	1.0

Date: Friday, August 28, 2009 Sheet 44 of 54



PM_LEVELDOWN#	1.8_OV	Voltage	Status
L	L	1.778V	Power Saving
H	L	1.803V	Normal
H	H	1.931V	Performance

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.7A
2. Ripple Current:
   I rip =2.72A
   I spec=2.5A
3. Dynamic:
   I peak=6.8A
   ESR / 1 pcs =18 mohm
   〉V =122.4mV
4. Inductor Spec:

I SAC=25.5A
IDC =15.5 A
DCR=5mohm

5. MOSFET Spec:

H-side MOSFET:RJK0355DPA-00-J0

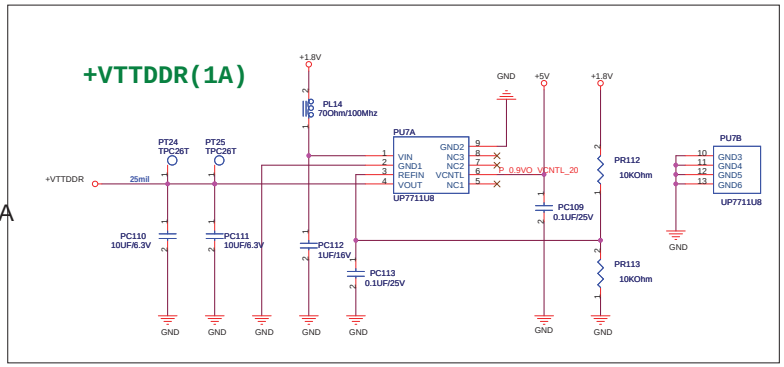
Rds(ON)= 16.5 mohm (Vgs=4.5 V)
I cont = 30 A (T =25)
I peak = 120 A (Pause ≦10 us)

L-side MOSFET: RJK0355DPA-00-J0

Rds(ON)= 16.5 mohm (Vgs=4.5 V)
I cont = 30 A (T =25)
I peak = 120 A (Pause ≦10 us)

Controller

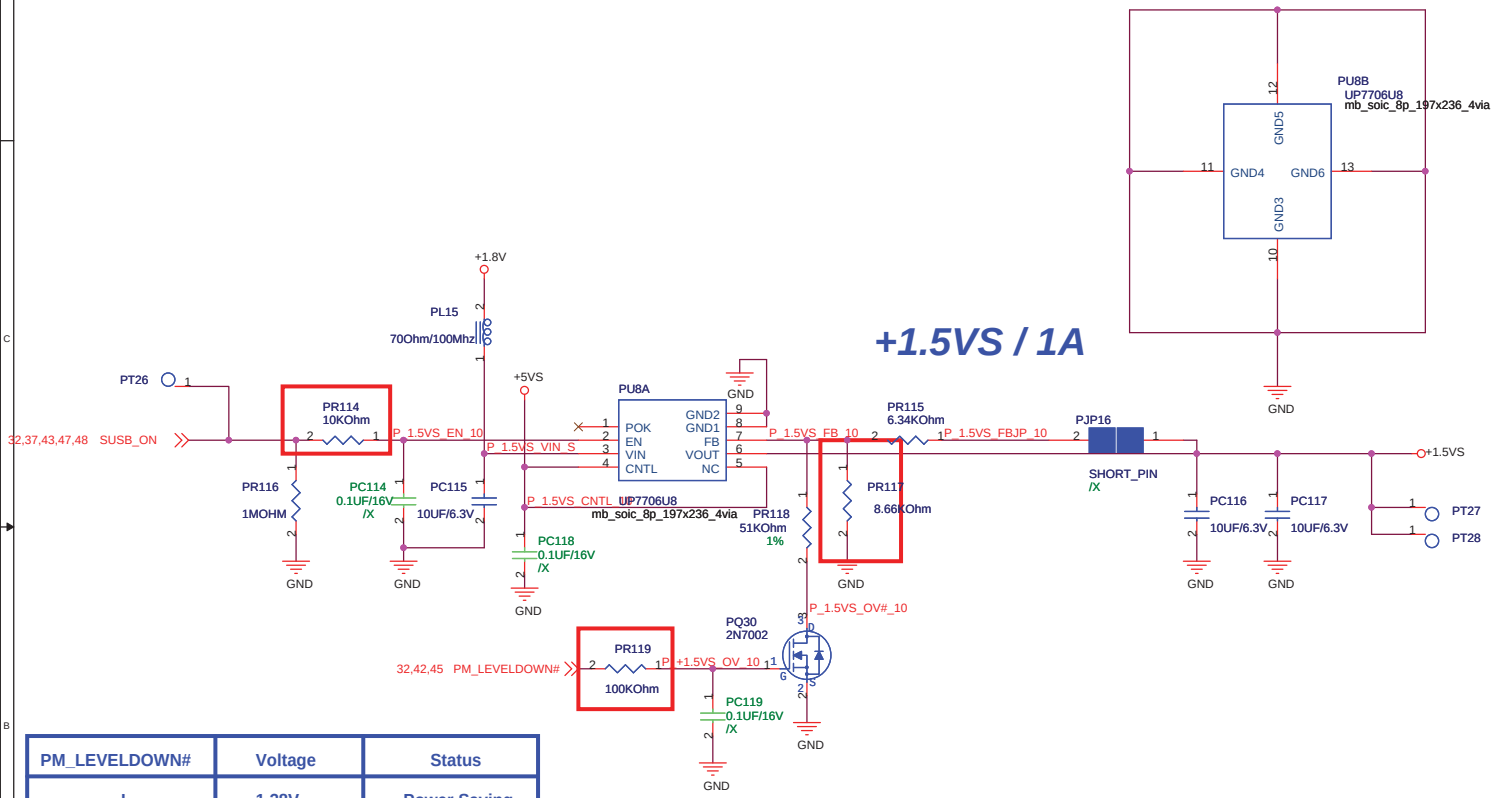
1. Voltage & Current:
   +1.8V@6.8A
2. Frequency:
   PR101=510Kohm
   Fosc=480KHz
3. OCP:
   PR102=15K ohm -> 18A
4. POR:
   Vccrth =3.7~4.1V
   Vcchys=0.2V
5. UVP:
   Vout*70%
6. OVP:
   Vout*115%
7. Enable Voltage:
   V = 2.9V
8. Soft start time:
   Tss=1.2 ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.15 A



0.9VS@1 A

1. Dropout Voltage:
   〉V = 0.3V (Io = 2 A)
2. Current Limit:
   I limit = 4 A
3. Continue Current:
   I cont = 3 A
4. Power Dissipation:
   Rthjc = 52 /W
   Pd = 1.9 W
5. EN Voltage:
   V en = 1.4V
   V sd = 0.8 V
6. Supply Voltage:
   Vcc = 5 V
7. Inrush current:
   T ss = 5 ms
   C total = 10 uF
   I inrush = 3 mA

ASUSTek Computer INC	Title : +1.8V&VTTDDR	
	Engineer: Joy_Zhou	
Size: A2	Project Name: 12011i	Rev: <RevCode>
Date: Friday, August 28, 2009	Sheet 45 of 54	

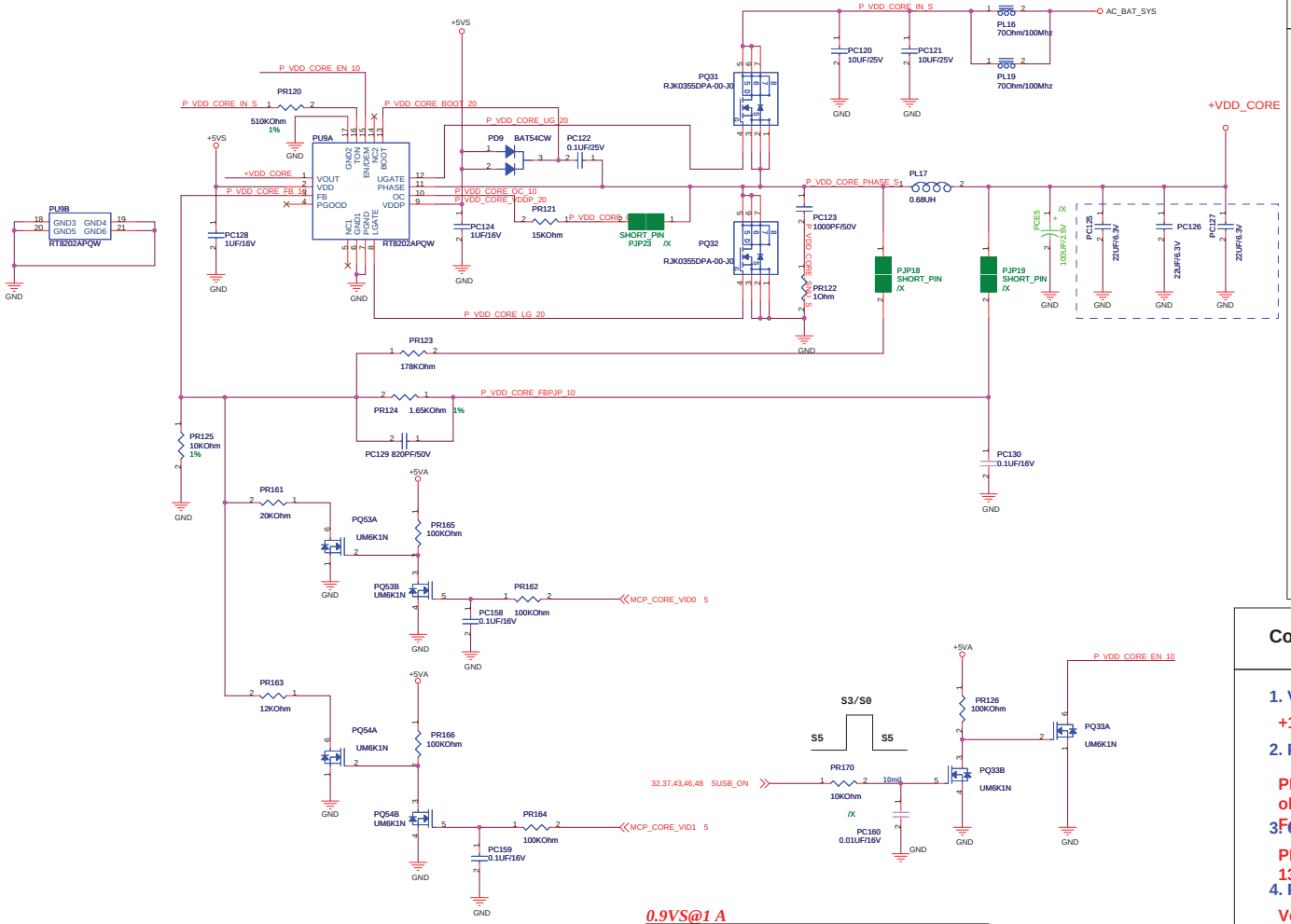


PM_LEVELDOWN#	Voltage	Status
L	1.38V	Power Saving
H	1.48V	Normal

1. Dropout Voltage:
   〉 V= 300 mV (Io=2 A)
2. Current Limit:
   I limit= 2.8 A
3. Continue Current:
   I cont= 1A
4. Pd:
   R thjc =5 C/W
   Pd =1.9W
5. EN Voltage:
   V rising = 1.4 V
   V falling = 0.4 V
6. Supply Voltage:
   Vcc=5V
7. Inrush current:
   Tss = 4 ms
   C total = 20 uF
   I inrush= 7.5mA

<Variant Name>

ASUSTek Computer INC.	Title : +1.5VS	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 1201i	Rev: 1.2
Date: Friday, August 28, 2009	Sheet 46 of 54	



Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.7A
2. Ripple Current:
   I rip =2.72A
   I spec=2.5A
3. Dynamic:
   I peak=6.8A
   ESR / 1 pcs =18 mohm
   〉V =122.4mV
4. Inductor Spec:

I SAC=25.5A
IDC =15.5 A
DCR=5mohm

5. MOSFET Spec:

H-side MOSFET: RJK0355DPA-00-J0

Rds(ON)= 16.5 mohm (Vgs=4.5 V)
I cont = 30 A (T =25)
I peak = 120 A (Pause ≦10 us)

L-side MOSFET: RJK0355DPA-00-J0

Rds(ON)= 16.5 mohm (Vgs=4.5 V)
I cont = 30A (T =25)
I peak = 120 A (Pause ≦10 us)

Controller

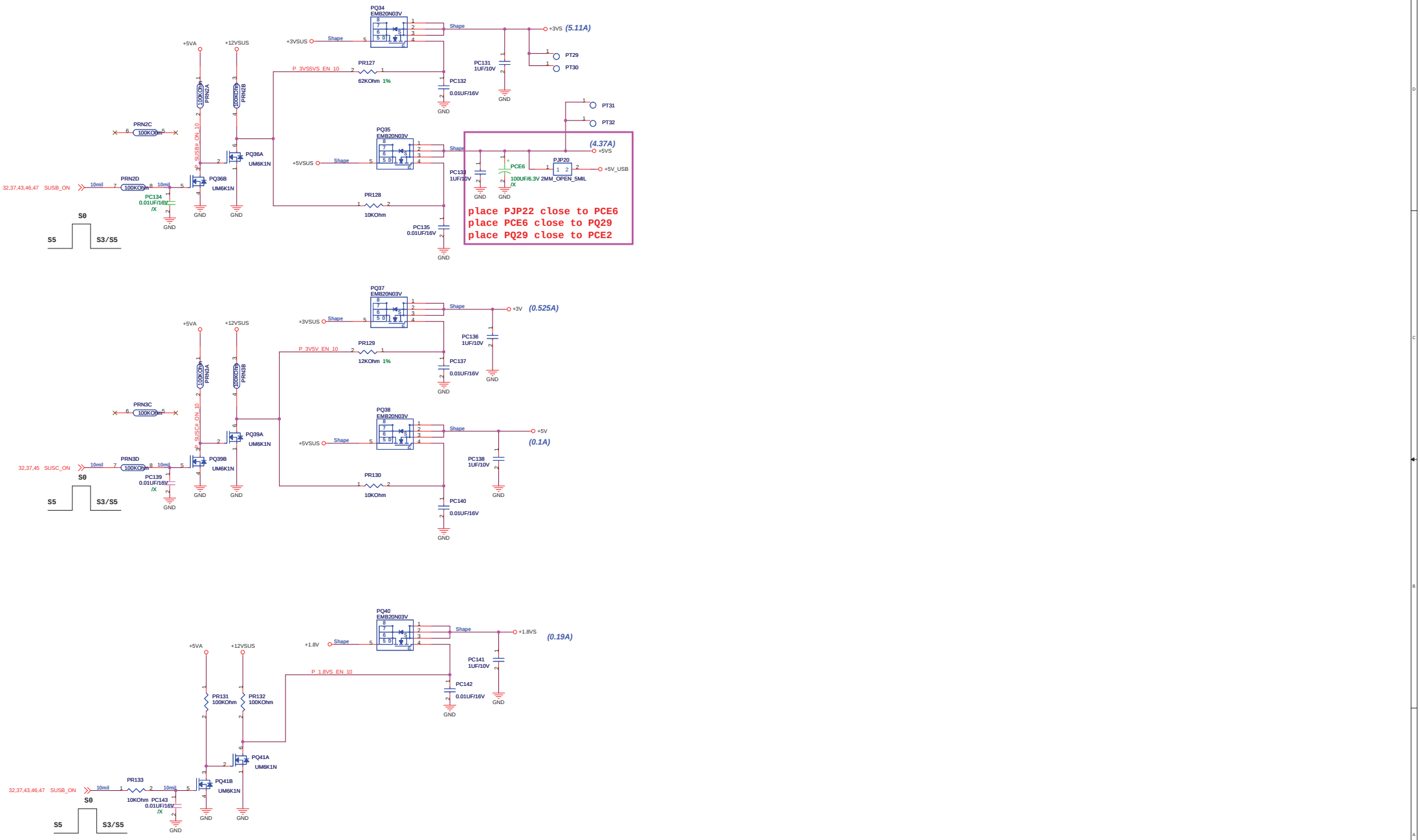
1. Voltage & Current:
   +1.8V@6.8A
2. Frequency:
   PR120=510K ohm
   Fosc=480KHz
3. OCP:
   PR121=18K ohm -> 13.6A
4. POR:
   Vccrth =3.7~4.1V
   Vcchys=0.2V
5. UVP:
   Vout*70%
6. OVP:
   Vout*115%
7. Enable Voltage:
   V = 2.9V
8. Soft start time:
   Tss=1.2 ms
9. Phase selection:
   /X
10. Inrush Current:
    C total = 100 uF
    I inrush= 0.15 A

0.9VS@1 A

1. Dropout Voltage:
   〉V = 0.3V (Io = 2 A)
2. Current Limit:
   I limit = 4 A
3. Continue Current:
   I cont = 3 A
4. Power Dissipation:
   Rthjc = 52 /W
   Pd = 1.9 W
5. EN Voltage:
   V en = 1.4V
   V sd = 0.8 V
6. Supply Voltage:
   Vcc = 5 V
7. Inrush current:
   T ss = 5 ms
   C total = 10 uF
   I inrush = 3 mA

VID2	VID1	VID0	Voltage	Status
L	L	L	0.88V	N/A
L	L	H	1V	Normal
L	H	L	0.95V	Performance
L	H	H	0.9V	Power Saving

ASUSTek Computer INC
Title : +1.8V&VTTDDR
Engineer: Joy_Zhou
Size: A2 | Project Name: 1201i | Rev: <RevCode>
Date: Friday, August 28, 2009 | Sheet 47 of 54



<Variant Name>

ASUSTek Computer INC.

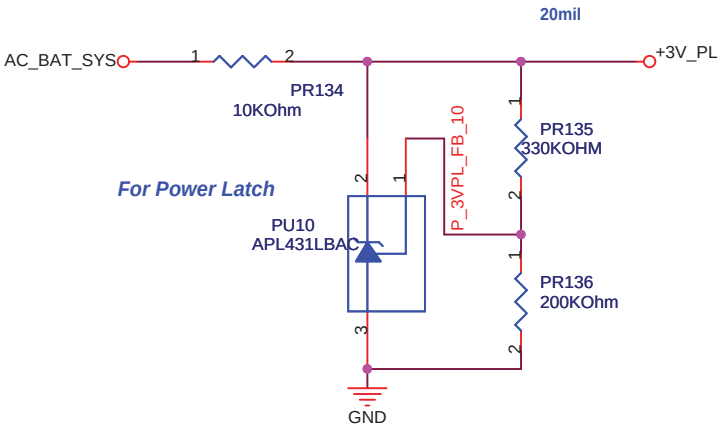
Title : Power_Load Switch

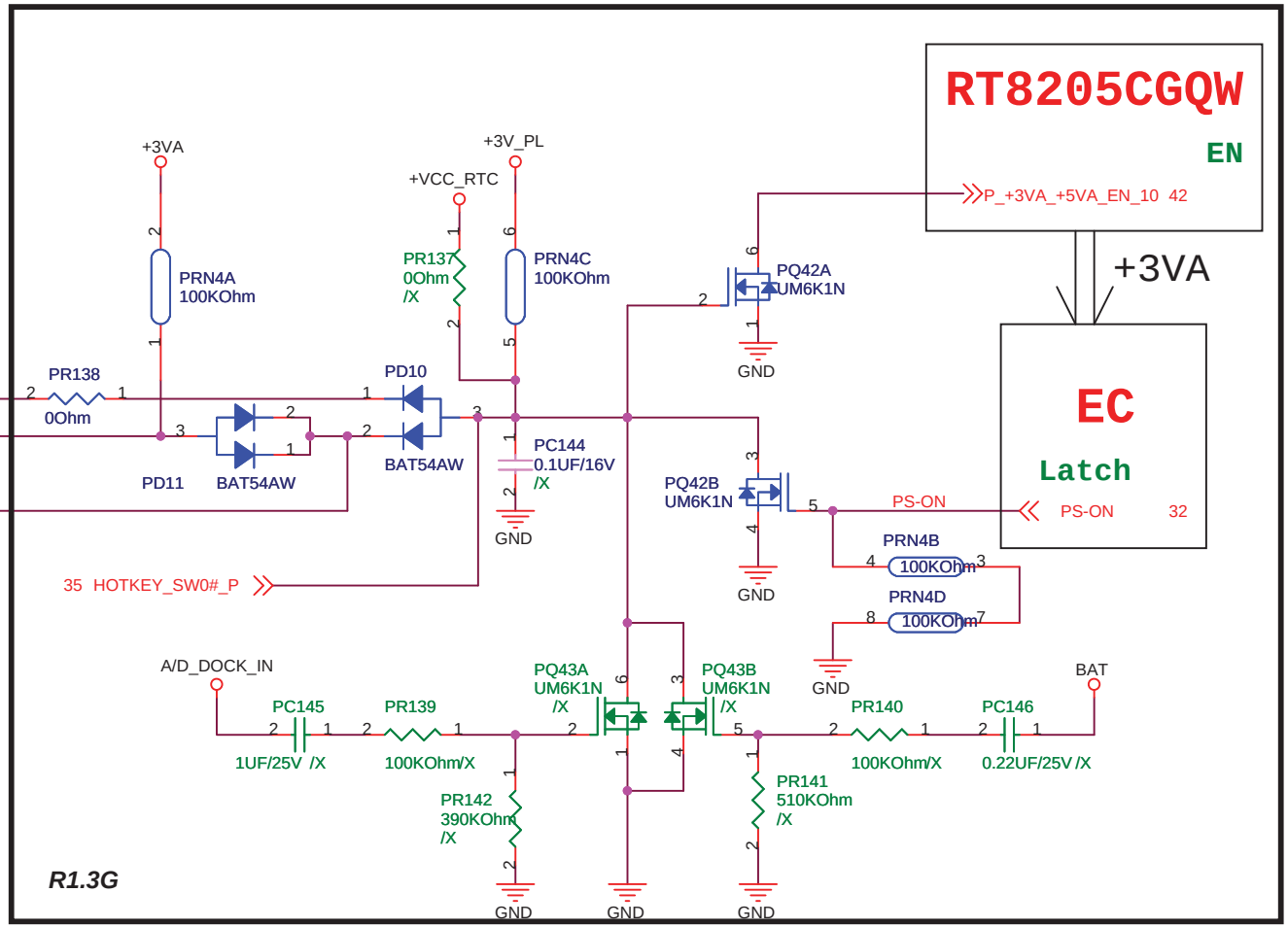
Engineer: Joy_Zhou

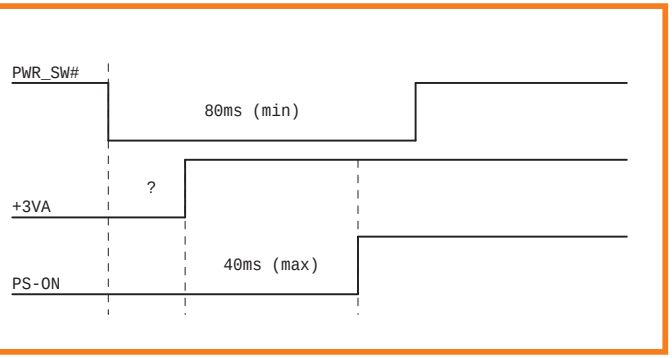
Size	Project Name	Rev
A2	12011	1.2

Date: Friday, August 28, 2009 Sheet 48 of 54

+3V_P L







<Variant Name>

ASUSTek Computer INC.	Title : Power Latch		
	Engineer: Jerry Liu		
Size: A4	Project Name: 1201i		Rev: 1.0
Date: Friday, August 28, 2009	Sheet 49 of 54		

<OrgName>	Title : HISTORY	
	Engineer: <OrgAddr1>	
Size: A3	Project Name: 1201HA	Rev: 1.0
Date: Friday, August 21, 2009	Sheet 50 of 54	

DATE 0706

1. P40,Delete some EMI CAP,add RF CAP EC58
2. P23,3G_RST# PU POWER change from +3VS to +3V_3G
3. P15,SCH_GPIO_0 PD R93 change from 10k to 1K
4. P16,+5VS_REF ADD serial R109
5. P22,+3V_LCD ADD GR15/PQ40
6. P23,+3V_3G GR21/GR22 change to 0805
7. P35,L26 change to 0 OHM
7. P7,CLK_PCIE_3G/CLK_PCIE_3G# add reserved CAP C476/C477

DATE 0707

1. P13,SDVO BUS/PCIE add net name before capacitor
2. P22,LVDS CON change part number to 12G17101020K
3. P40, add EMI CAP EC52/EC54
3. P29, add power switch for debug

DATE 0708

1.Delete test point T27/T28
2.ADD D6/OR30
3.Add net name for PCIE BUS

<OrgName>	Title : HISTORY	
	Engineer: <OrgAddr1>	
Size A3	Project Name 1201HA	Rev 1.0
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EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	LPC_RST#	I	
14	GPIO07	CRT_IN	I	100K pull high to +3VA
15	GPIO08	EXT_SMI#	O	
16	GPIO0A	LID_EC_R#	I	Internal pull high
17	GPIO0B/ESB_CLK	PCB_ID0	I	8.2K pull down to GND
18	GPIO0C/ESB_DAT	PCB_ID1	I	8.2K pull down to GND
19	GPIO0D	LID_EC_L#(no use)	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	O	10K pull high to +3VSUS
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#(no use)	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	100K pull high to +3VSUS
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM(no use)	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH(no use)	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX(no use)	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX(no use)	I	RS232 debug port
32	GPIO18	PWR_SW_EC#	I	100K pull high to +3VA
34	GPIO19/PWM3	PS-ON	O	latch power, 200K pull down to GND
36	GPIO1A/NUMLED	NUM_LED#(no use)	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#(no use)	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A(no use)	I	
64	GPI39/AD1	BAT_B(no use)	I	
65	GPIO3A/AD2	BAT_C(no use)	I	
66	GPIO3B/AD3	BAT_D(no use)	I	
68	GPO3C/DA0	CHG_EN#	O	100K pull high to +3VA
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	Default High
72	GPO3F/DA3	BAT_LL#(NO USE)	O	Battery Low Low
73	GPIO40	AC_OK	I	100K pull high to +3VA
74	GPIO41	EC_RSMRST#	O	100K pull down to GND
75	GPI42	BAT_IN	I	100K pull high to +3VA
76	GPI43	BAT2_IN(no use)	I	Batt1 (Small/Internal): 1 present, 0 absent (to GND)
77	GPIO44/SCL1	SMB1_CLK	I/OD	4.7K pull high to +3VA
78	GPIO45/SDA1	SMB1_DATA	I/OD	4.7K pull high to +3VA
79	GPIO46/SCL2	SMB2_CLK	I/OD	10K pull high to +3VS
80	GPIO47/SDA2	SMB2_DATA	I/OD	10K pull high to +3VS
81	GPIO48/KSO16	KB_ID0(no use)	I	for KB type detection
82	GPIO49/KSO17	KB_ID1(no use)	I	for KB type detection
83	GPIO4A/PSCLK1	1.8_OV	O	10K pull down to GND; default low
84	GPIO4B/PSDAT1	NC	I	
85	GPIO4C/PSCLK2	NC	O	
86	GPIO4D/PSDAT2	NC	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3VS
88	GPIO4F/PSDAT3	TP_DATA	I/OD	10K pull high to +3VS
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_ORANGE#	O	Orange charger LED
91	GPIO53/CAPLED	CAPS_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#(no use)	O	
95	GPIO56	GS1_INT1(no use)	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON_EC	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#(no use)	O	
103	GPXOA06	PM_LEVELDOWN#	O	Default High
104	GPXOA07	CNT2_CHG#(no use)	O	
105	GPXOA08	CNT2_CHG#(no use)	O	
106	GPXOA09	SPI_WP#	O	10K pull high to +3VA
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	100K pull down to GND
109	GPXID0/SDIDI	EC_PWROK	O	100K pull down to GND
110	GPXID1	CPU_LEVELUP#	O	Default High
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SUSB#	I	100K pull down to GND
115	GPXID4	PM_SUSC#	I	100K pull down to GND
116	GPXID5	VRM_PWRGD_EC	I	100K Pull high to +3VS
117	GPXID6	VSUS_PWRGD	I	100K Pull high to +3VA
118	GPXID7	NC	O	
121	GPIO57	GS1_INT2(no use)	I	Internal pull high
126	GPIO58/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_KBCLPC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
87	ECRST#	EC_RST#	I	100K pull high to +3VA
67	AVCC	+3VA_AEC	P	
69	AGND	GND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_DO	I	
120	WR#/SPIDO	SPI_DI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	K_V18R	P	Reserved 4.7uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

<Variant Name>

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: N/A

Size	Project Name	Rev
A3	1201HA	1.0

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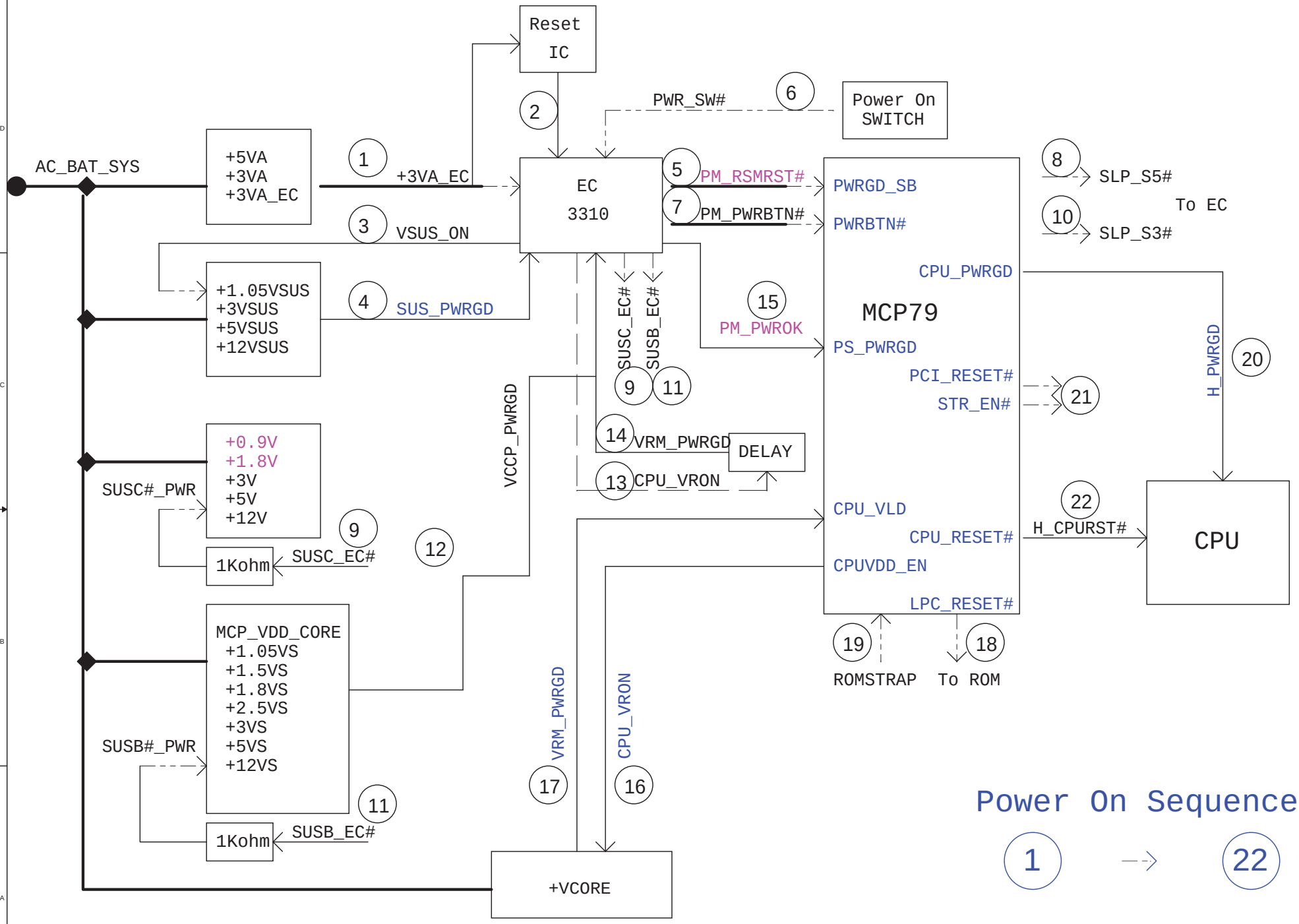

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ASUSTeK COMPUTER INC		Title : PowerOn sequence	
		Engineer: MIRO TSAI	
Size: Custom	Project Name: 1201I		Rev: 2.0g
Date: Wednesday, July 29, 2009		Sheet 53 of 54	

S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for AC_OK until adaptor power is good, then

2.At least 5mS after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.

3.At least 20mS after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)

4.EC asserts RSTWARN.

5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

6.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

7.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

8.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

10.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

11.Waiting for RSTRDY# until deasserted by SCH.

12.RESET# can be deasserted at lease 100uS after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for BAT_IN until battery power is good, then

2.Waiting for PWR_SW# until user is pressed.

3.EC asserts VSUS_ON to enable VSUS power.

4.At least 20mS after VSUS power is stable.

5.EC asserts RSTWARN.

6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.

10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

12.Waiting for RSTRDY# until deasserted by SCH.

13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).

2.At least 20mS after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.

3.Waiting for SLPRDY# until has been asserted.

4.EC asserts RSTWARN to SCH to begin internal sequence.

5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.

6.EC asserts RESET# after detecting RSTRDY# asserted.

7.EC deasserts ICH_PWROK.

8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

9.EC asserts PM_RSMRST#.

10.EC deasserts SUSC_ON to turn off the other power planes.

11.EC deasserts VSUS_ON if in battery mode.

12.EC deasserts RSTWARN to save more power.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.

2.For external wake event (PWR_SW#, keyboard wake up), then

3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.

4.EC asserts SUSB_ON to enable SUSB power.

5.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

7.At least 5mS after receiving CPUPWR_GD, ICH_PWROK is asserted.

8.Deasserts RSTWARN after ICH_PWROK is asserted.

9.RESET# can be deasserted 100uS after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.

2.EC asserts RSTWARN to SCH.

3.EC asserts RESET# for 1200mS to SCH after asserts RSTWARN.

4.EC deasserts RSTWARN.

5.EC deasserts RESET# after at least 100uS delay from RSTWARN.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.

2.EC asserts RSTWARN to SCH.

3.EC asserts RESET# to SCH after asserts RSTWARN.

4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.

5.EC asserts PM_RSMRST# after CPU_VRON power is off.

6.EC disables SUSC_ON power for 3~5 seconds.

7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.